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THESIS

DESIGN OF A LOW POWER EMBEDDED MICROPROCESSOR FOR A HANDS-EYES-EARS-FREE PERSONAL NAVIGATION AND COMMUNICATIONS SYSTEM

by

Peter H. Haase

June 2000

Thesis Advisor: Douglas J. Fouts

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DESIGN OF A LOW POWER EMBEDDED MICROPROCESSOR FOR A HANDS-EYES-EARS-FREE PERSONAL NAVIGATION AND COMMUNICATION SYSTEM

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ABSTRACT

This thesis details the engineering design of a personal, computer-based system, which is intended to support a hands-eyes-ears-free Personal Navigational and Communication System (PNCS). This computer-based system is designed to be used with COTS devices, such as, (1) a GPS receiver, (2) a laptop or desktop computer, (3) a rechargeable, long-life battery pack, and (4) a wearable tactile communications vest. The vest is currently under development by the Naval Aerospace Medical Research Lab (NAMRL) and together with this computer-based system can provide a complete hands-free personal navigational and communication system. The intent of the navigation system is to satisfy both commercial and military uses for land-based pedestrian and vehicular travel.

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SYMBOLS, ACRONYMS, AND ABBREVIATIONS

BIOS	Basic Input Output System
CEP	Circular Error Probable
CMOS	Complementary Metal Oxide Semiconductor
COTS	Commercial Off-The Shelf
C_{PD}	Power Dissipation Capacitance
DGPS	Differential Global Positioning System
DMA	Direct Memory Access
DoD	United States Department of Defense
DOS	Disk Operating System
DRAM	Dynamic Random Access Memory
EIA	Electronic Industries Association
EIA-232	Standardized Unbalanced Asynchronous Serial Communications Protocol
EEPROM	Electrically Erasable Programmable Read Only Memory
ESR	Equivalent Series Resistance
FET	Field Effect Transistor
FLASH	Non-Volatile, Electrically Block Erasable, Programmable Memory
FTL	File Translation Layer
GDOP	Geometric Dilution of Precision (GPS)
GPS	Global Positioning System
HDOP	Horizontal Dilution of Precision (GPS)
Hz	Hertz
I_{CC}	Operating Supply Current
ISA	Industry Standards Association
JEDEC	Joint Electronic Devices Engineering Council
KB	10^3 Bytes

kph	Kilometers Per Hour
LCD	Liquid Crystal Display
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
mA	10^{-3} Amps
mAh	10^{-3} Amp * Hours
MHz	10^{6} Hertz
mm	10^{-3} Meters
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
mph	Miles Per Hour
ms	10^{-3} Seconds
NAMRL	Naval Aerospace Medical Research Lab, Florida
NiCad	Nickel Cadmium
NiMH	Nickel Metal Hydride
NSWCDD	Naval Surface Warfare Center Dahlgren Division, Dahlgren, VA
ONCE	ON Circuit Emulation
OS	Operating System
PCB	Printed Circuit Board
PDOP	Position Dilution of Precision (GPS)
PNC	Personal Navigation and Communication
PNCC	Personal Navigation and Communication Computer
PNCS	Personal Navigation and Communication System
POST	Power On System Test
PPS	Precise Positioning System
PROM	Programmable Read Only Memory
RAM	Random Access Memory
RMS	Root-Mean-Square (one Standard Deviation)
ROM	Read Only Memory
RTCM	Radio Technical Committee, Marine

SA	Selective Availability (GPS)
SEP	Spherical Error Probable
SRAM	Static Random Access Memory
SV	Space Vehicle
TDOP	Time Dilution of Precision (GPS)
TIA	Telecommunications Industry Association
TSAS	Tactile Situational Awareness System
TTL	Transistor-Transistor Logic
mA	10^{-3} Amps
µS	10^{-6} Seconds
pF	10^{-12} Farads
µP	Microprocessor
UVPROM	Ultra-Violet Erasable Programmable Read Only Memory
V	Volts
VAC	Alternating Current Voltage
V_{cc}	Operating Supply Voltage
VDC	Direct Current Voltage
VDOP	Vertical Dilution of Precision (GPS)
VGA	Video Graphic Array

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TERMINOLOGY

A number of terms referenced in this document are defined here for clarity.

3V System This term generally refers to chips or circuits that are designed to operate in the range of 3.3 volts ± 0.3 volts. This coincides with the JEDEC standard for regulated power supplies [Ref 1].

5V System This term generally refers to chips or circuits that are designed to operate in the range of 5.0 volts ± 0.5 volts. This coincides with the JEDEC standard for unregulated power supplies [Ref 1].

C_{PD} Power Dissipation Capacitance. An equivalent capacitance used to determine the power dissipation of an integrated circuit device.

Crystals: Drive Level Specifies the maximum power dissipation for which the manufacturer calibrated the crystal [Ref 2].

Crystals: Equivalent Series Resistance (ESR) ESR is proportional to crystal thickness, inversely proportional to frequency [Ref 2].

Crystals: Resonance and Load Capacitance Crystals carry a parallel or series resonance specification. The two types do not differ in construction, just in test conditions and expected circuit application [Ref 2].

Crystals: Temperature Range Specifies an operating range over which the crystal's frequency will not vary beyond a stated limit [Ref 2].

Crystals: Tolerance The allowable frequency deviation at a particular calibration temperature, usually 25° C. Standard microprocessor crystals typically have a frequency tolerance of 0.01% (100 parts per million, ppm), these crystals are ideal for the 80C186 Modular Core family [Ref 2].

Crystals: Vibration Mode The vibration mode is either fundamental or third overtone. Crystal thickness varies inversely with frequency. Vendors furnish third or higher overtone crystals to avoid manufacturing very thin, fragile quartz crystal elements [Ref 2].

GPS: Geometric Dilution of Precision The volume of the shape described by the unit-vectors from the receiver to the SVs used in a position fix is inversely proportional to GDOP. GDOP is computed from the geometric relationships between the receiver position and the positions of the satellites the receiver is using for navigation.

GPS: L-Band The L-Band is the portion of the electromagnetic spectrum used for the transmission of GPS data streams. The L-Band is divided into two carrier frequencies, L-1 and L-2, which are 1575.42 MHz and 1227.60 MHz respectively. The carrier frequencies are phase modulated over a 1 MHz band by three different binary codes to provide the SPS, PPS, and Navigation Message data.

GPS: Precise Positioning System The Precise Positioning System (PPS) is that portion of the GPS which provides authorized users with a precise positioning capability. The Federal Raidonavigation Plan publishes the PPS predictable accuracy as 22-meter horizontal accuracy, 27.7-meter vertical accuracy, and 100-nanosecond time accuracy.

GPS: Standard Positioning System The Standard Positioning System (SPS) is that portion of the GPS which provides "civil users" with a degraded version of the Precise Positioning System (PPS) offered by the GPS. The Federal Raidonavigation Plan publishes the accuracy of the SPS as 100 meter horizontal, 156 meter vertical, and 340 nanosecond time accuracy.

Power Regulators: Dropout Voltage The regulators minimum input-output voltage differential. This determines the lowest usable supply voltage [Ref 3].

Selective Availability A process implemented by the Department of Defense for deliberately obscuring the position of a GPS satellite by continuously altering the satellites on-board real-time clock with near random "corrections."

Spatial Disorientation The loss of orientation with respect to a geographic reference. In this context, pilots experiences spatial disorientation when they loose track of their reference to ground. If this happens, the pilot seriously runs the risk of flying into the ground.

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I. INTRODUCTION

A. OBJECTIVE

The objective of this Thesis is to provide the engineering design of a personal computer, which is intended to support a hands-eyes-ears-free Personal Navigational and Communication System (PNCS). This computer is designed to be used with COTS devices, such as, (1) a GPS receiver, (2) a laptop or desktop computer, (3) a rechargeable, long-life battery pack, and (4) a wearable tactile communications vest. The vest is currently under development by the Naval Aerospace Medical Research Lab (NAMRL) and can provide a complete hands-free personal navigational and communication system. The intent of the navigation system is to satisfy both commercial and military uses for land-based pedestrian and vehicular travel. Figure 1 is a conceptual diagram of the proposed Personal Navigation and Communication System (PNCS).

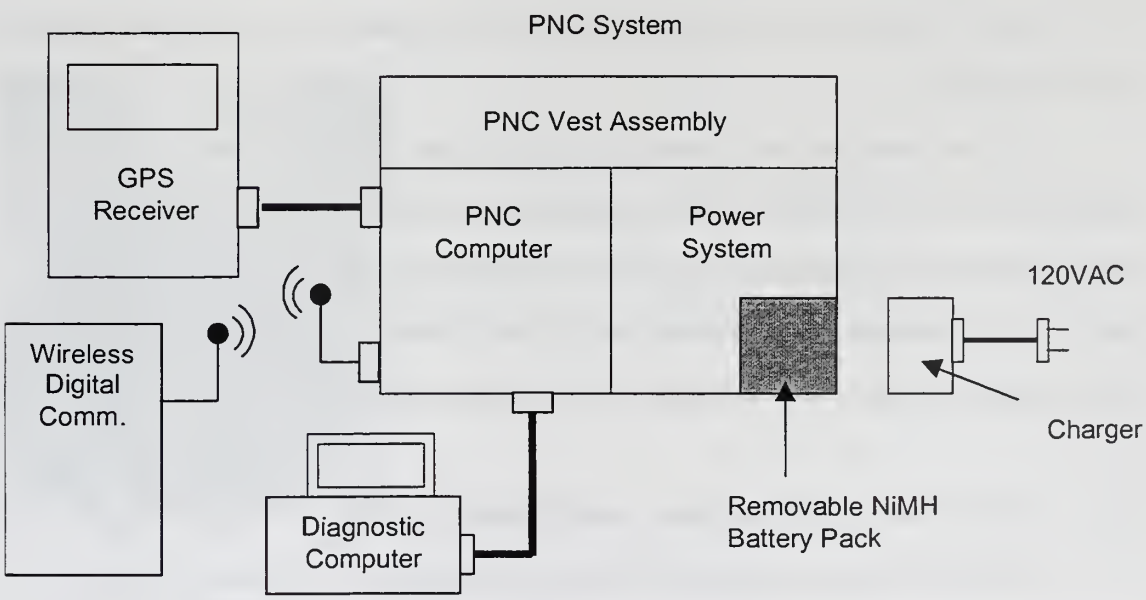

Figure 1. Conceptual View of the Personal Navigation and Communication System.

This thesis focuses on the design of the computer and its supporting subsystems. Specifically, this thesis addresses (1) the embedded microprocessor, (2) the memory, (3) the

communication interfaces, and (4) the power supply. This thesis does not address (1) specifics regarding the selection and use of GPS receivers, (2) development of software for the PNCS, or (3) the design of a tactor based vest.

B. BACKGROUND

As our technology and ability to produce faster and more capable aircraft improves, our human pilots in modern aircraft face the growing problem of spatial disorientation [Ref 4]. The Naval Aerospace Medical Research Laboratory (NAMRL) in Pensacola, Florida has engaged an effort to solve this problem. The NAMRL has undertaken to develop a Tactile Situational Awareness System (TSAS). The objective of the TSAS is to reduce pilot error by providing the pilot with an accurate continuous flow of information about the attitude of the aircraft with respect to ground. However, the system must not add to the pilot's already stressed levels of visual and auditory sensory input. Therefore, this system is designed to stimulate the under-utilized tactile sense. The TSAS uses an array of vibrotactile stimulators in concert with the aircraft's onboard instrumentation to provide a non-visual and non-auditory representation of the aircraft's attitude and orientation.

This technology can be adapted for numerous other applications. Some of these applications include (1) underwater spatial awareness and navigation, (2) orbital extravehicular spatial awareness and navigation, (3) control of unmanned vehicles (UAV), (4) flight simulator training, (5) and terrestrial communication and navigation [Ref 4]. This thesis will focus on this last application of tactile stimulus, terrestrial communication and navigation.

C. THE UNITED STATES GLOBAL POSITIONING SYSTEM

The United States Department of Defense has deployed and maintains an array of satellites for the purpose of providing a precise, continuously available navigation tool [Ref 5]. This system is called the United States Global Positioning System (GPS). The GPS costs approximately $400 Million per year and is currently estimated to cost approximately $6.5 billion in total assets. The technology behind the GPS is fairly simple. Twenty-four active GPS

satellites are in orbit approximately 11,000 miles from the surface of the earth. These satellites transmit signals which are received by land-borne GPS receivers. The receivers can determine the distance to the satellites by measuring the travel time of each signal. A receiver can determine its position (i.e. latitude, longitude, altitude, and time) on or near the earth by having line of sight access to at least four of these satellites. The basic GPS service provided by the DoD provides 100 meter accuracy 95% of the time.

The GPS is typically broken down into three segments. These segments are typically referred to as (1) the space segment, (2) the control segment, and (3) the user segment. The space segment consists of 24 satellites orbiting the earth in six different orbital planes. These satellites typically include solar panels, four atomic clocks accurate to one nanosecond, various radio transmitters, and several antennas. The GPS signals are transmitted on L-Band antennas. Because the US military deployed the system, the GPS data is transmitted in two different forms, one form for military use and the other for civilian use. The civilian signals are deliberately obscured through a process referred to as selective availability.

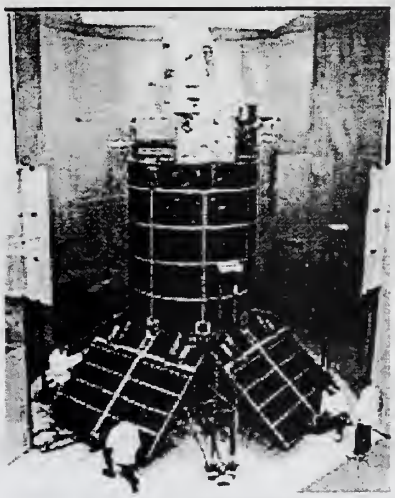

Figure 2. GPS Satellite.

The Control Segment of GPS consists of a master control station, several monitoring stations, and ground antennas. The master control station, located in Colorado Springs, is responsible for overall management of the remote monitoring and transmission sites. As the

center for support operations, it calculates any position or clock errors for each individual satellite based on information received from the monitor stations and then "orders" the appropriate ground antennas to relay the requisite corrective information back to that satellite. Each of the monitor stations checks the exact altitude, position, speed, and overall health of the orbiting satellites. A station can track up to 11 satellites at a time. This "check-up" is performed twice a day by each station as the satellites complete their journeys around the earth. Noted variations, such as those caused by the gravity of the moon and sun and the pressure of solar radiation, are passed along to the master control station. Ground antennas monitor and track the satellites from horizon to horizon. They also transmit correction information to individual satellites. These components enable the U.S. Air Force to collect satellite data pertaining to orbital position and satellite health and then transmit necessary corrections and maintenance information back to the satellites. Figure 3 shows the locations of GPS control and monitoring stations around the world.

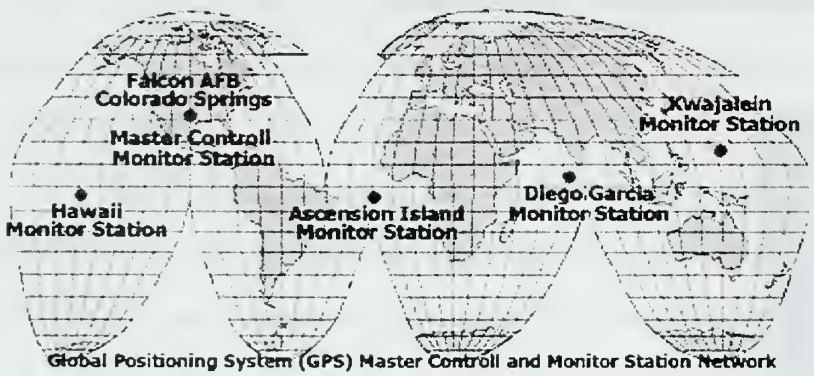

Figure 3. GPS Control Map.

The user segment consists of the entire population of the world. The US DoD is currently operating under the March 26, 1996, Presidential Decision Directive which mandates that GPS signals be provided to the civilian population. As a result, navigators equipped with GPS receivers use satellites as precise reference points to triangulate their positions for all kinds of navigation needs ranging from aircraft, to naval, to hikers.

1. GPS Error Sources

Error sources for GPS receivers can be divided into three categories, noise, bias, and blunders. Noise errors are typically introduced through errors in the generation of the L-Band signals and through the electronics inherent in the GPS receiver. These errors are typically small, around one or two meters. Bias errors are introduced through a variety of means including Selective Availability, tropospheric delays, ionospheric delays, and multipath ambiguity [Ref 5]. Blunders represent human errors or just plain mistakes.

2. Selective Availability

The Federal Raidonavigation Plan (FRP) has established two variants of GPS data. These variants are the Standard Positioning Service (SPS) and the Precise Positioning Service (PPS). The PPS is provided for authorized users such as the U.S. and allied military and some specially approved civilian users. The published accuracy of the PPS is 22 meter Horizontal accuracy, 27.7 meter vertical accuracy, and 100 nanosecond time accuracy. The SPS is provided for civilian users world wide without charge. The accuracy of the SPS is 100 meter horizontal accuracy, 156 meter vertical accuracy, and 340 nanoseconds time accuracy.

Selective Availability (SA) is the intentional degradation of the Standard Positioning Service (SPS) signals by a time varying bias. SA is controlled by the DoD to limit accuracy for non-U. S. military and government users. The potential accuracy of the code of around 30 meters is reduced to 100 meters (two standard deviations). The SA bias on each satellite signal is different, and so the resulting position solution is a function of the combined SA bias from each Space Vehicle (SV; aka satellite) used in the navigation solution. Because SA is a changing bias with low frequency terms in excess of a few hours, position solutions or individual SV pseudo-ranges cannot be effectively averaged over periods shorter than a few hours. Differential corrections must be updated at a rate less than the correlation time of SA (and other bias errors). For more details on selective availability and the GPS code see [Ref 5].

3. Differential GPS (DGPS)

Differential GPS, or DGPS, is a system for improving the accuracy of GPS receivers by correcting for Selective Availability as well as environmental error sources. This is accomplished through the use of "base stations" that measure the errors and then "broadcast" the corrections to GPS receivers. The broadcasts are usually made in the form of microwaves for short ranges, low frequencies for medium ranges, geostationary satellites for long ranges. Some systems also use cellular telephone downlinks. DGPS corrections can also be post-processed for applications that do not require real-time updates.

There are two main error sources for which DGPS is capable of correcting. These are (1) Selective Availability and (2) environmental errors introduced by the ionosphere and/or the troposphere. Of these error sources the most significant by far are those introduced by Selective Availability. The base station compensates for SA in the following way. The base station knows its precise measured location. It also determines the locations of each GPS satellite within its field of view by using the ephemeris that is the normal broadcast message from all GPS satellites. The base station calculates the range to each satellite based on this information and then compares those ranges to its known measured location. The difference between the *computed* range and the *measured* range is the *range error*. In addition to computing the range error for each satellite, the base stations also calculate a *range rate* or the "range error rate of change." Because most radio transmission systems are bandwidth limited, including the range rate allows DGPS capable GPS receivers to employ a kind of dead reckoning in between DGPS updates.

The environmental errors introduced by the ionosphere and troposphere are typically small, errors of up to 10 meters, and somewhat constant for a given area. These areas can be quite large, on the order of several hundred miles in diameter. The most effective way for a GPS receiver to eliminate this error is to use DGPS range errors broadcast from "local" (with in several hundred miles) base stations.

4. DGPS Solutions: OmniStar

A variety of solutions exist for collecting DGPS data. DGPS data can be gathered for post-processing of GPS data for systems that do not require real time updates. For systems requiring real time updates, corrections are typically received through one form or another of broadcast or in some cases through cellular connections.

One method for a user to obtain DGPS corrections is through a contract with a vendor such as OMNISTAR. OMNISTAR is a company established to provide DGPS corrections to users through the use of distributed base stations and geo-stationary satellite transmissions. The OMNISTAR system was designed for (1) continental coverage, (2) sub-meter accuracy over the entire continental coverage, and (3) portability. The OMNISTAR coverage area covers southern Canada, all 48 states of the United States, and the northern half of Mexico with sufficient power that a small omni-directional antenna may be used to receive the DGPS corrections from a geo-stationary satellite. Figure 4 is a graphical representation of the OMNISTAR coverage area.

The OMNISTAR network consists of ten permanent base stations that are scattered throughout the Continental US, plus one in Mexico. These stations track all GPS Satellites above 5 degrees elevation and compute corrections every 600ms. These corrections are transmitted to a Network Control Center (NCC) located in Houston, Texas, via leased lines, in the industry standard format RTCM-104 Version II. The NCC checks, compresses, and formats the incoming data from the 11 base stations into a packet for transmission to the satellite every 2 to 3 seconds. The satellite uses spread spectrum transmissions to broadcast the data back out to all OMNISTAR DGPS capable receivers. The receivers decode the spread spectrum data and decompress the packet.

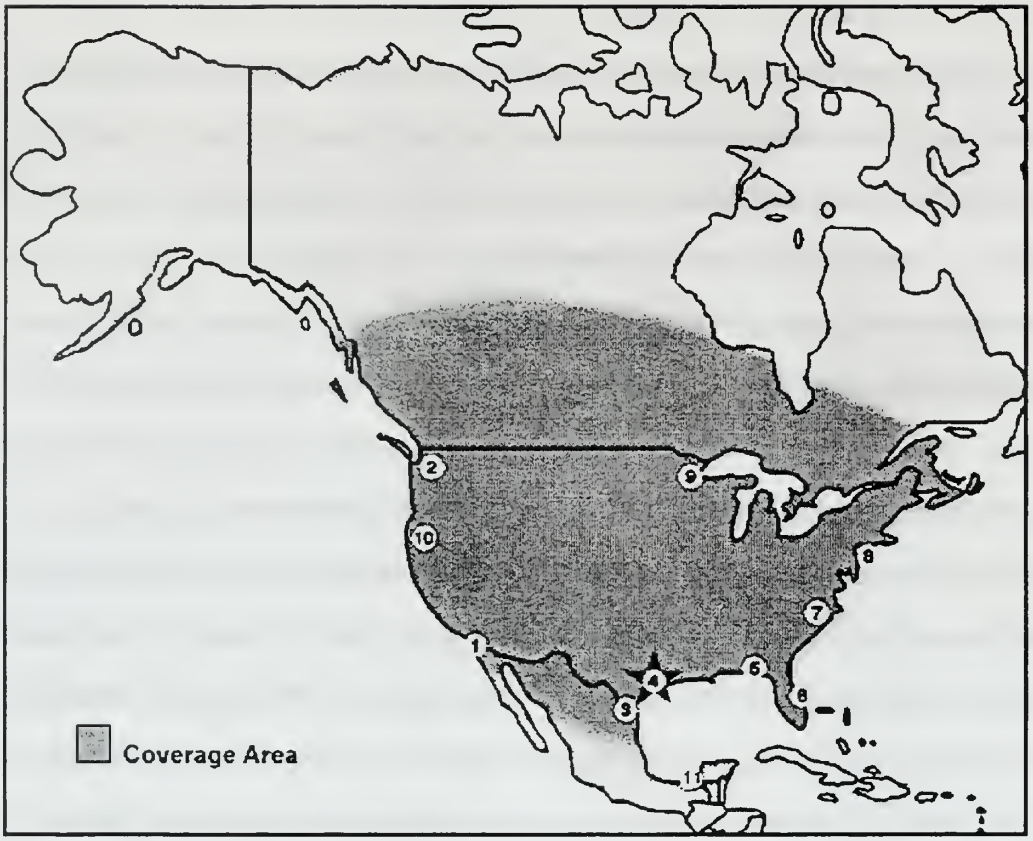

Figure 4. OMNISTAR DGPS Satellite Coverage Area [Ref 6].

The packet is then corrected for atmospheric errors. The DGPS receiver corrects for the atmospheric errors by knowing its approximate location to within 50 or 100 miles. The DGPS receiver typically does this automatically by collecting a location from the GPS receiver (even if the GPS receiver's location is only accurate to within 100 meters). Figure 5 summarizes how the Omnistar system works. First GPS satellites transmit uncorrected data to the ground. The nationally deployed Omnistar base stations determine real-time errors in the signals and transmit the corrections to an Omnistar satellite uplink. The Omnistar satellite then transmits the corrections to all Omnistar equipped receivers.

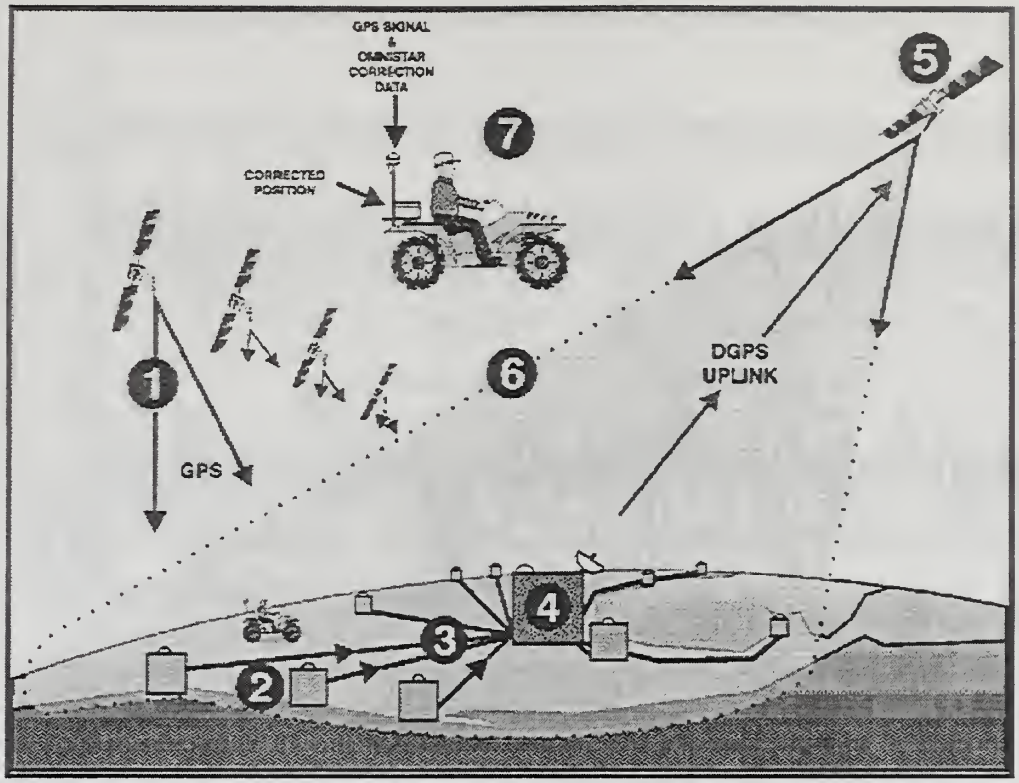

Figure 5. How the OMNISTAR DGPS System Works [Ref 6].

OMNISTAR performed a series of tests to gather data about the effectiveness of their DGPS system. Their first step was to capture some baseline information about the behavior of non-differentially corrected systems. Figure 6 shows the results of collecting data over a 24-hour period. The figure shows three plots of data. The first is the Horizontal Dilution Of Precision (HDOP), which is a calculated measure of the uncertainty of the horizontal position fix. The second is the actual east/west error denoted as ΔE and given in meters. The last plot is the actual north/south error denoted as ΔN and also given in meters. From this information it is clear that (1) the errors change continuously, (2) the rate of change is relatively slow, (3) the errors appear to be random, (4) the errors approach a zero mean over a long period of time, and (5) the one sigma values are quite high with a 3 sigma value on the order of 17.6m * 3 = 42.8m. Meaning that 99.5% of the time an uncorrected GPS system will read an accurate position to within about 43 meters of it's true position. However, if the data is collected over a long period of time, the position fix can be expected to be accurate to within about 1.0 meters.

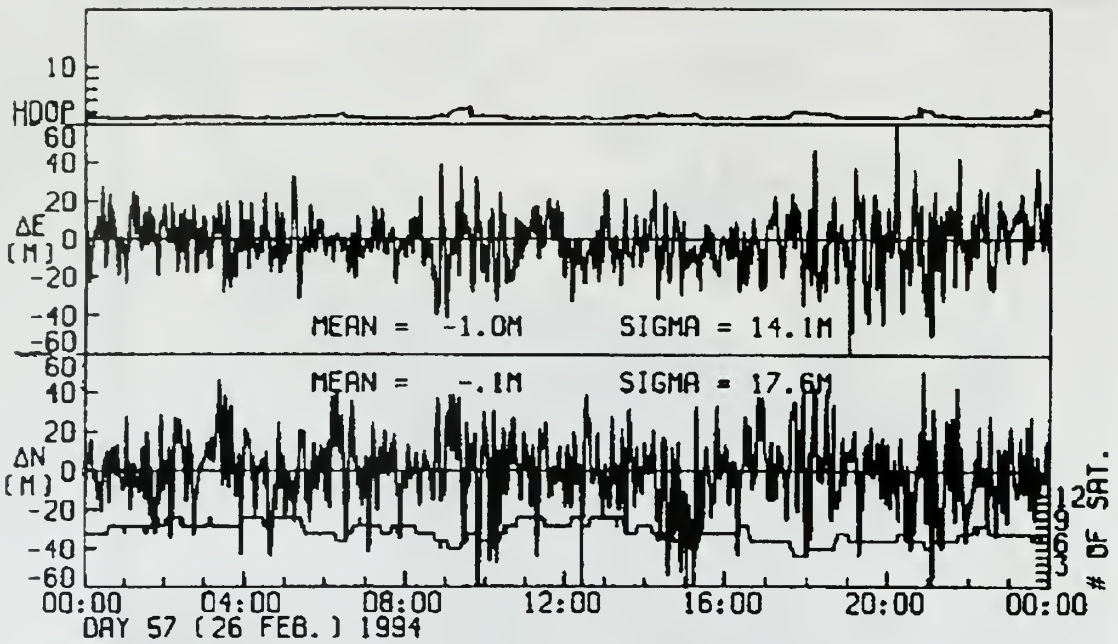

Figure 6. "24 Hour" Error Plot of "Non-Differential" GPS Data.

To illustrate the effect of the environmental delays, differential correction information was applied to the same non-differential data plotted in Figure 6. The differential correction data was obtained from a single differential base station located in Cocoa Beach, Florida. The non-differential data was collected in Houston, Texas. The interesting findings from this data are (1) a clear improvement (approximately one order of magnitude) in the one sigma ΔE and ΔN and (2) a clear shift in the ΔE and ΔN mean data. This shift is the offset introduced by the atmospheric errors. Figure 7 shows the differentially corrected plots.

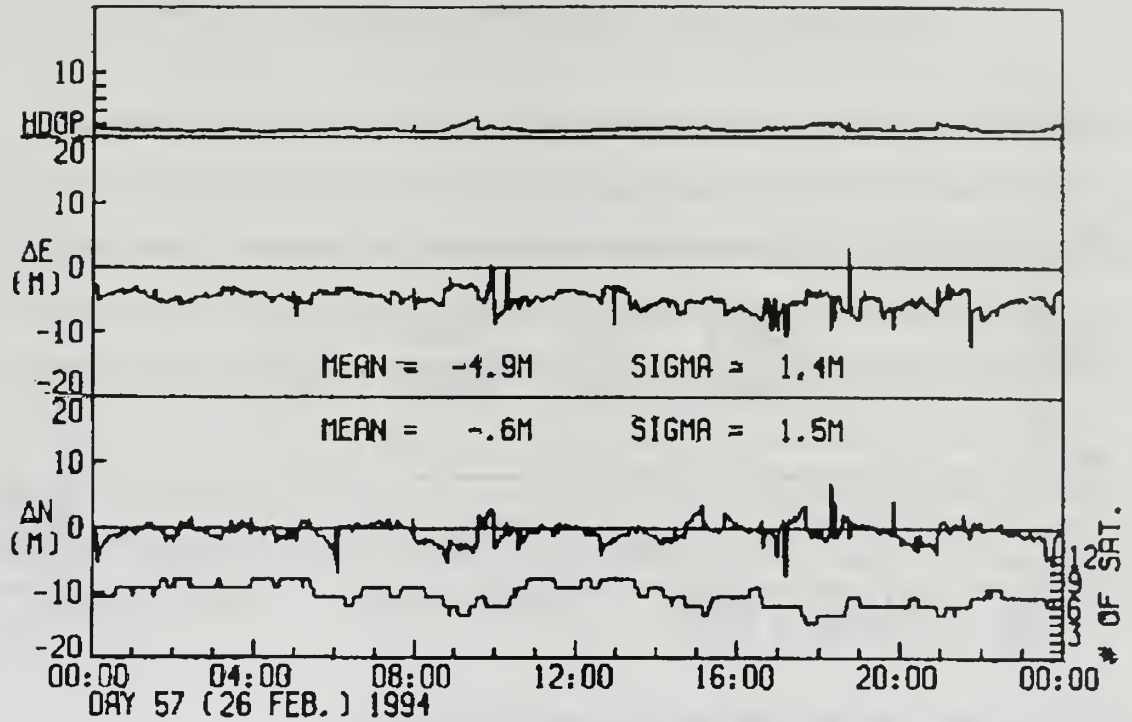

Figure 7. Corrected GPS Data using DGPS corrections from Cocoa Beach, FL.

The base station compensates for these errors at it's location but not at the remote GPS receivers location. Figure 8 illustrates the effect of using three different base stations to compute the range error. These data show the ability to obtain GPS position fixes with sub-meter accuracy 99.5% of the time [Ref 6].

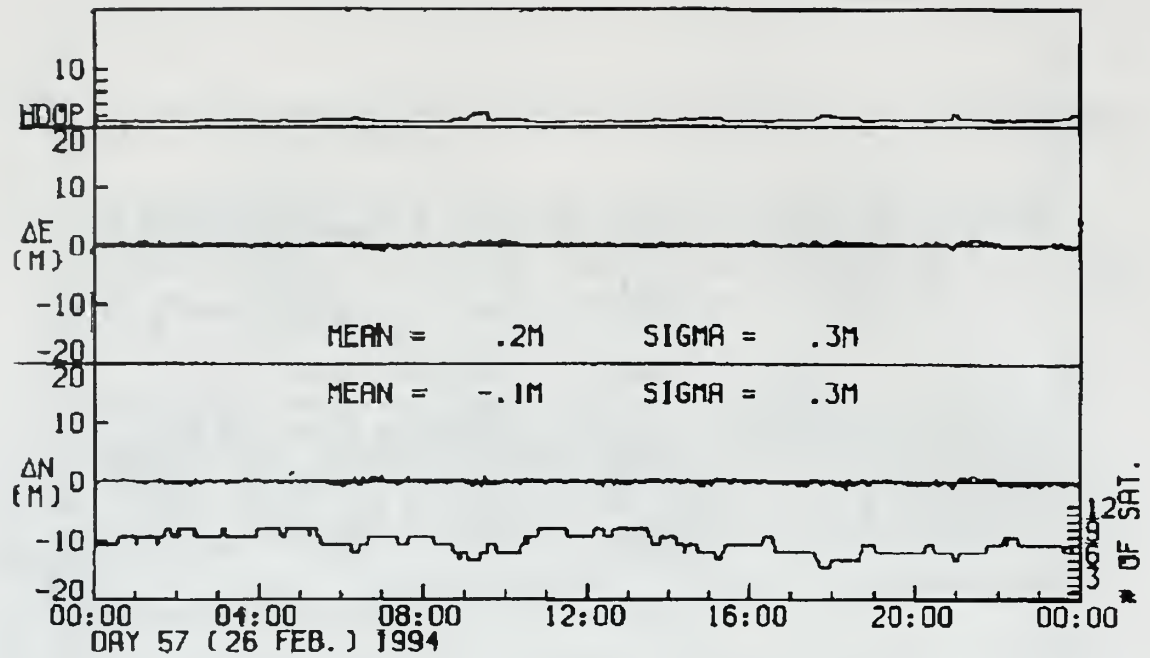

Figure 8. DGPS Corrected GPS Data using three base stations.

The OMNISTAR service typically consists of an initial hardware procurement and a subsequent service contract. The hardware procurement is the acquisition of an OMNISTAR DGPS receiver. This receiver is capable of receiving and decoding the OMNISTAR satellite transmissions and performing the local corrections for atmospheric errors. This receiver is also equipped with an industry standard interface for connecting to a DGPS capable input on any one of a number of "standard" GPS receivers. OMNISTAR provides DGPS receivers for costs that range between $2,875.00 to $5,500.00. The DGPS service contract is typically written to cover a one year service contract for approximately $800 per year.

II. PNCC OBJECTIVES & REQUIREMENTS

Before the design of the PNCC can begin the designer must have a clear picture of the need that the PNCC will be filling. Therefore, this section will identify the objectives of the PNCS and then attempt to distill a set of top-level requirements for the "system." Requirements for the computer will then be defined based on the system requirements. The computer requirements will then drive the design of the computer. It is important to note, however, that this thesis is not devoted to the development requirements and their flow-down. It is, rather, focused on the design of an embedded microprocessor computer. Therefore, these requirements will not be explored in greater detail. They are only supplied here to facilitate the engineering based design of the PNCC.

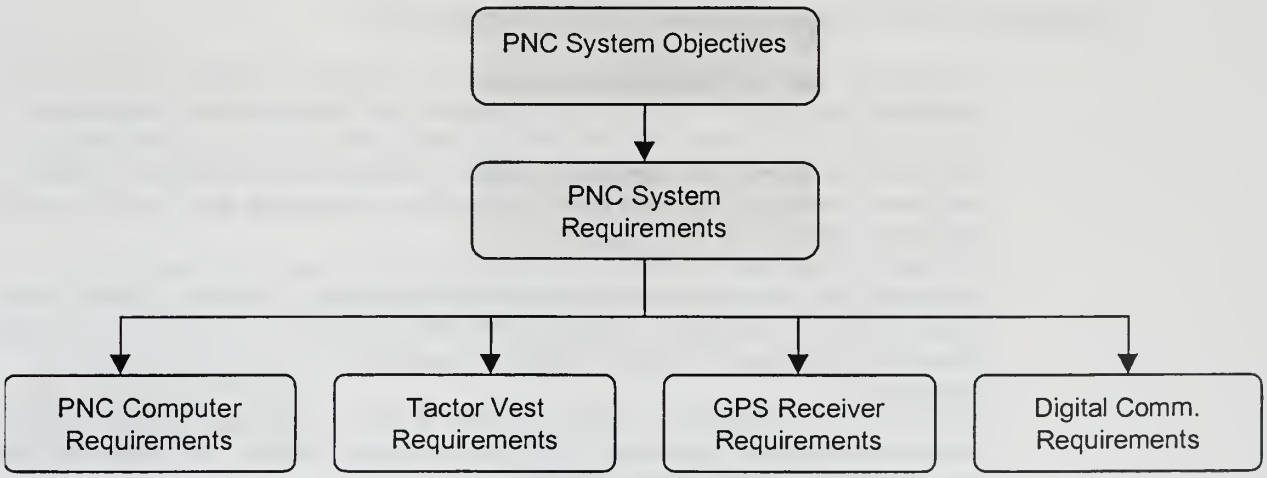

Figure 9. Requirements Flow of the PNC Computer.

A. OBJECTIVES

1. Personal Navigation and Communication System (PNCS) Objective

The objective of the PNCS is to provide a battery powered hands-eyes-ears-free personal navigational tool that does not require a significant portion of the user's attention. This

system is intended for use in conjunction with COTS GPS receivers and an array of up to eight Naval Aerospace Medical Research Laboratory (NAMRL) tactors.

2. Personal Navigation and Communication Computer (PNCC) Objective

The objective of the PNCC is to support the PNCS by providing a programmable interface between the COTS GPS receiver and/or a COTS digital radio, an array of up to eight NAMRL tactors, and a COTS laptop/diagnostic computer.

B. REQUIREMENTS

The requirements for both the PNCS and the PNCC stem from the respective objectives and are broken down by level. The primary requirements are defined as follows.

Navigational and Communication System (PNCS) Requirements

1. The system must be wearable and portable. The PNCS is intended to be worn by a human for the purpose of supplying navigational and communication information during travel. This means that the PNCS must be small enough and light enough that it may be worn by the "average" human for extended periods of time. It must also allow freedom of movement and function for a reasonable length of time under continuous use.
2. The system must be marketable. The equipment is dual use and commercial availability will reduce the acquisition costs to the military. Therefore, certain other issues should be considered when designing the equipment. For example, it should use rechargeable batteries and a battery charger that are readily available to the consumer.
3. Support COTS interfaces. It must be capable of communicating with any number of common peripherals, specifically, GPS receivers, digital radios, and laptop computers via a common communications protocol.
4. Support a "User Friendly" interface for configuration and use.

Personal Navigational and Communications Computer (PNCC) Requirements

The PNCC requirements are defined to support the PNCS requirements. The PNCC requirements are as follows.

1. Light Weight & Compact
2. Battery Powered
3. Support at least two simultaneous EIA-232 communication interfaces
4. Provide "current status" information to the user.
5. Allow "on-the-fly" system re-configuration.

6. Run for a minimum of 8 hours on continuous battery power
7. Capable of updating the user once every 500mS
8. Capable of driving up to eight tactors
9. Optional – Should be rechargeable

The following sections will describe the design of various elements of the PNCC. The elements include (1) the power system, (2) the microprocessor, (3) the memory subsystem, (4) the BIOS and OS, (5) the User Interface, (6) the GPS interface, (7) the external computer/diagnostic interface, (8) and the Tactor interface.

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III. PNCS OVERVIEW

This section provides a high level functional description of the PNCS. This section details the different components of the system and describes how each component interfaces with other components. Figure 10 is a functional diagram of the PNCS. It shows the functional relationships between the individual components of the entire system. This thesis deals only with the components that make up the PNCS Computer Assembly. Note that the peripheral component interfaces, such as the GPS interface, the digital communications equipment interface, the diagnostic computer interface, and the NAMRL Tactor vest interface, are included as part of the PNCS Computer Assembly.

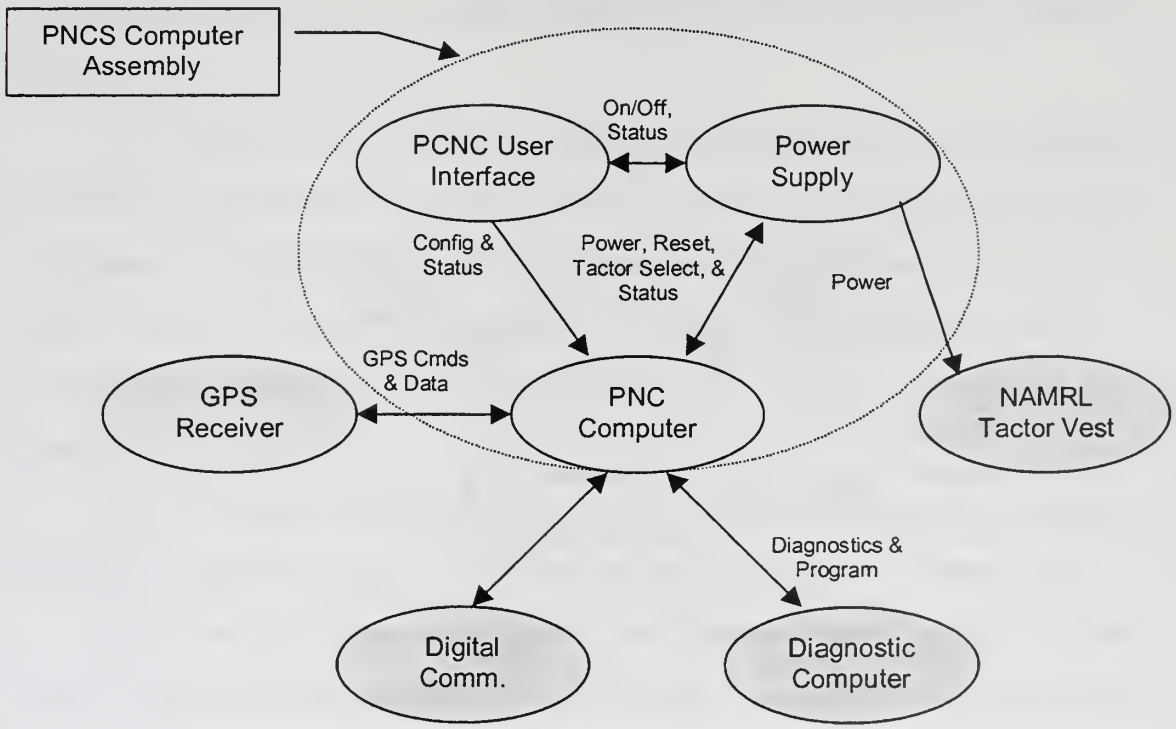


Figure 10. Functional Diagram of the PNC System.

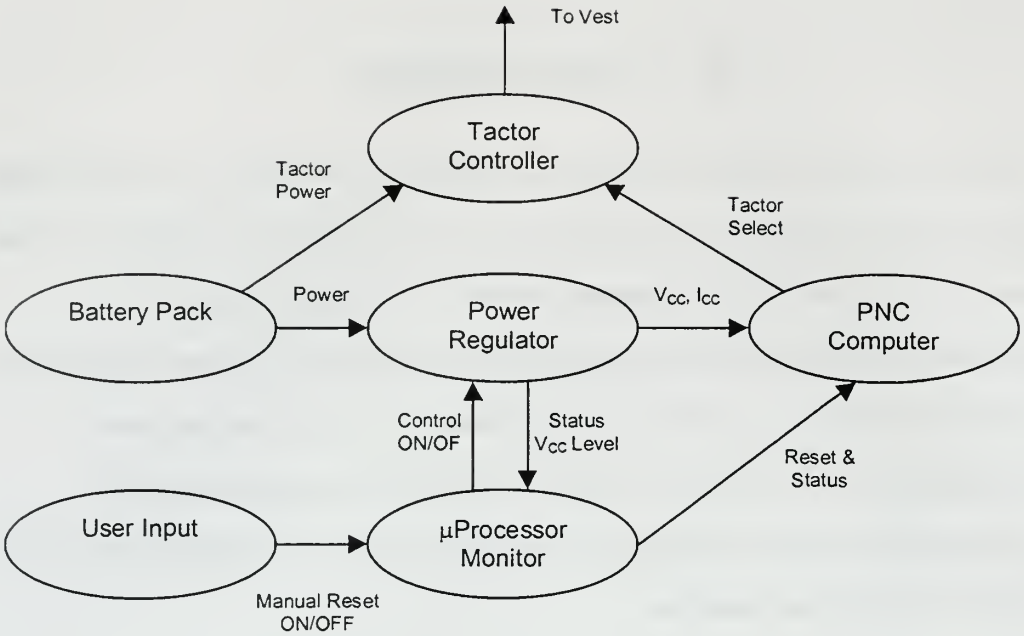


Figure 11. Functional Diagram of the Power Supply.

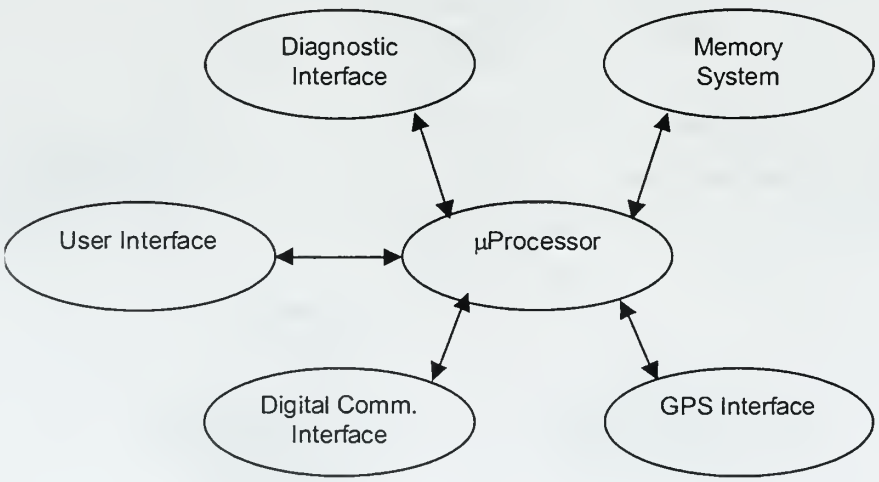


Figure 12. Functional Diagram of the PNC Computer.

IV. POWER SUPPLY DESIGN

A. INTRODUCTION

The power supply is probably the most critical component of this design. The requirements for the PNC System define that it must be portable. Therefore, the PNC Computer must be battery powered and light weight. These two requirements are the primary influence on the power system design. A pure 3V system design was chosen to limit power (and current) consumption and to extend battery life. A pure 3V system also reduces overall system weight by requiring fewer, and potentially smaller, batteries. Some chip manufacturers are currently developing components that will operate using lower voltages. For example, Samsung currently has some SRAM chips in development that use operating voltages between 1.8 and 2.7 volts. Once these chips become available under a production basis, they should be considered for low power applications such as this one.

The current capacity and characteristic voltage discharge curves of various batteries (i.e. NiCad, NiMH, and alkaline) combined with the need of some of the components requirements for a fairly stable operating voltage (i.e. 3.0v +/- 0.3v) may require the design to include a power regulation subsystem. The use of a regulator will cost the system more current but may also prolong the life expectancy of the batteries by maintaining the appropriate voltage level for a longer time.

For a more detailed cost/benefit analysis of low voltage embedded systems, see Intel Corporation's Application Note-477, *Low Voltage Embedded Design* by John Williams [Ref 1].

For this design, the power supply performs two primary functions. The first is to provide the PNCC with a constant and stable source of power. The second is to drive the tactors in the tactor vest. The PNCC will use six of its programmable I/O pins to send tactor control information to the tactor control circuit. The tactor control circuit will then drive the appropriate tactor(s). See APPENDIX B – CIRCUIT SCHEMATICS for a diagram of the tactor control circuit. The user program, to prevent the need for additional decoding hardware in the power supply, will handle

the tactor address decoding. This reduces both the cost and the power consumption of the entire system and increases the systems expandability.

B. BATTERY POWERED OPERATION

Battery operated device design requires the designer to consider (1) device operating voltage, (2) battery current capacity, (3) size restrictions, and (4) weight limitations. This section will focus on the first two considerations, device operating voltage and current capacity. In general, batteries do not hold a constant voltage or current supply over their lifetime. The two types of batteries of most interest are alkaline batteries, for the relatively high current capacity, and rechargeable (Nickel Cadmium and Nickel Metal Hydride), for their more stable voltage discharge profile. We will also only concern ourselves with the commonly available, COTS, sizes (i.e. AAA, AA, C, D, etc.).

Alkaline batteries typically generate 1.5 volts and have much greater current capacity (mAh) per unit volume than other kinds of batteries, with the exception of lithium batteries. However, the voltage output of alkaline batteries can vary greatly during its operational lifetime. Rechargeable batteries like Nickel-Cadmium (NiCad) and Nickel-Metal Hydride (NiMH) do not have the current capacity of alkaline batteries. However, their voltage discharge profiles are better suited to the battery-operated designs of microprocessors. Figure 13 and Figure 14 below show the differences between the voltage discharge profiles of alkaline and NiMH batteries.

Lithium batteries have the best of both worlds. They have greater current capacity and they have a better discharge profile (i.e. they hold a higher voltage for a longer duration). Figure 15 provides a comparison of the various batteries.

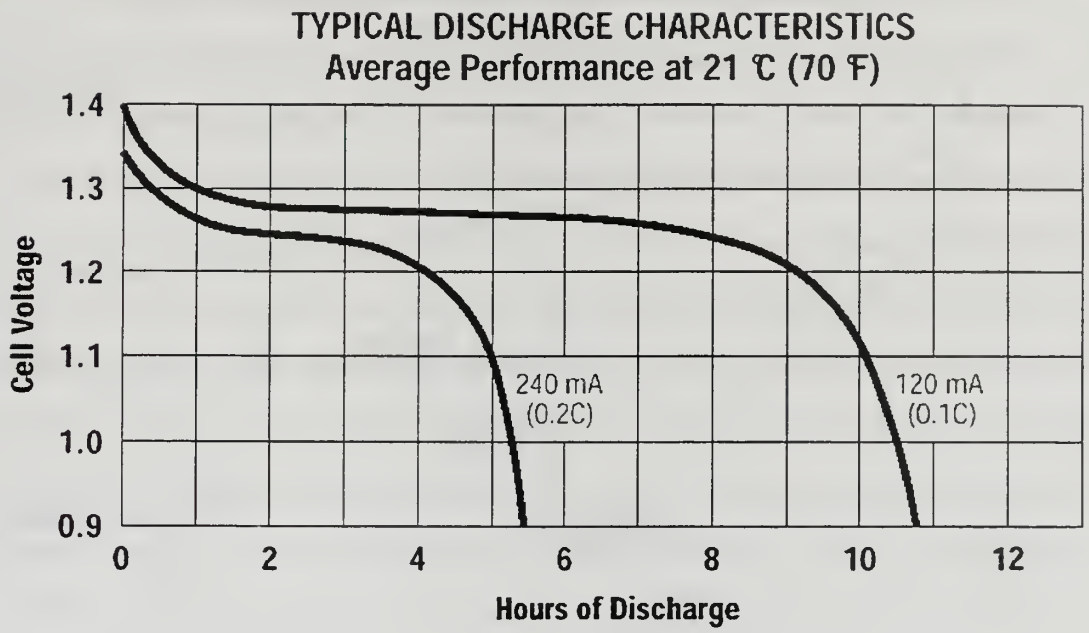


Figure 13. Typical Discharge Characteristics of Duracell NiMH batteries [Ref 7].

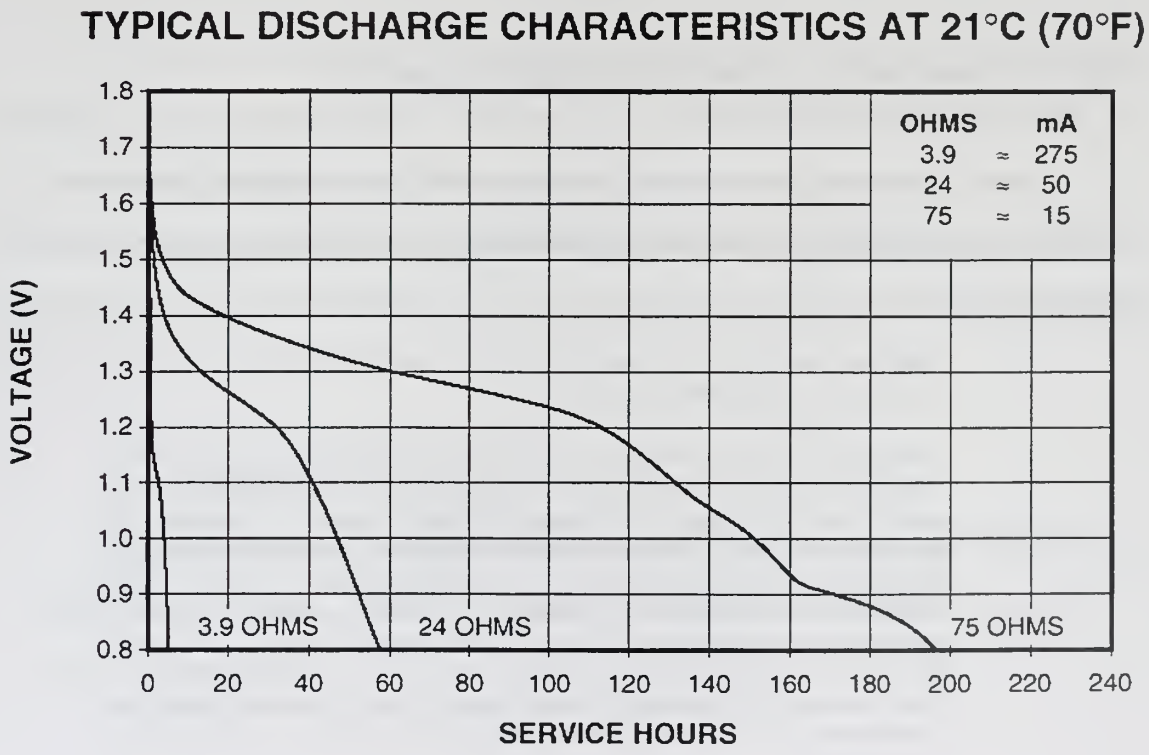


Figure 14. Typical Discharge Characteristics of Eveready Alkaline Batteries [Ref 8].

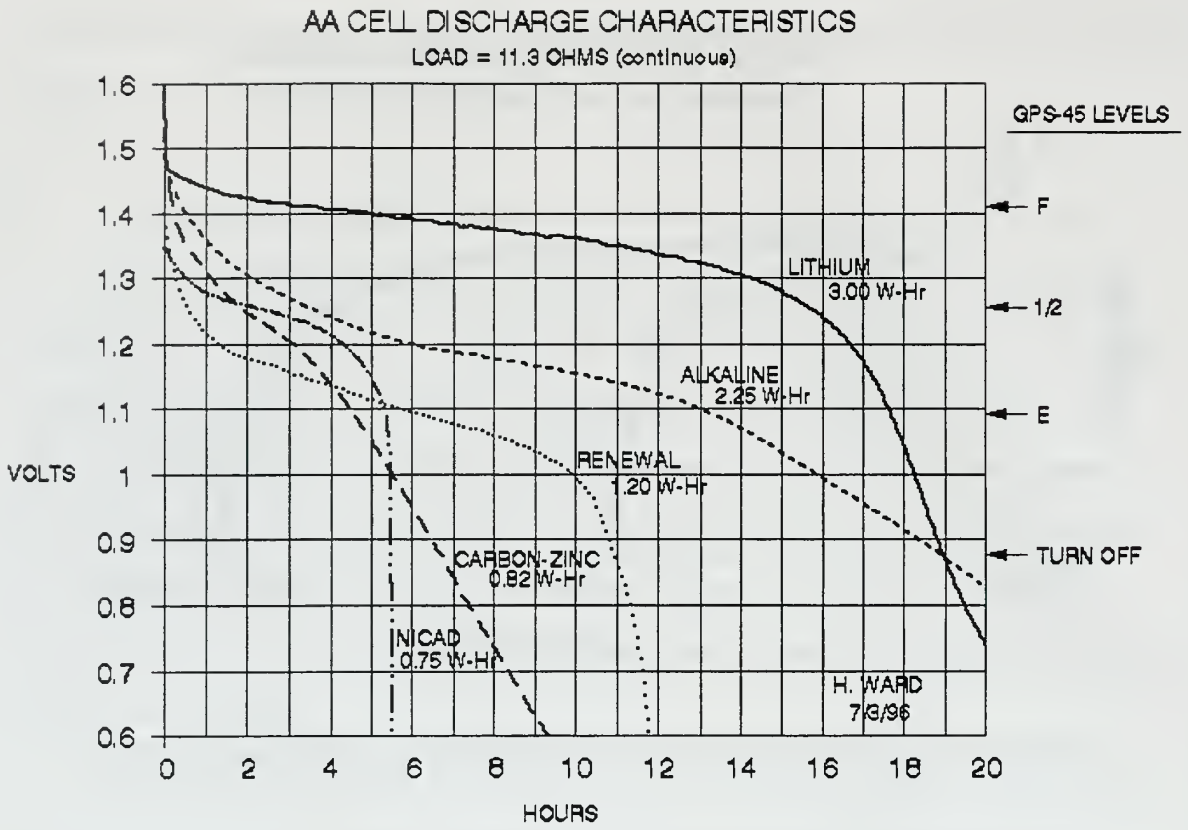


Figure 15. Comparison of AA Battery Discharge Characteristics.

Figure 15 depicts a comparison of discharge curves between various types of AA batteries. This information was compiled and presented by Garmin Industries with the following text caption.

> *BATTERY DISCHARGE DATA*
>
> *The graph shows the voltage as a function of time for various AA cells then continuously loaded by a 11.3 ohm resistor. This resistance approximates the load of the Garmin GPS-45 receiver. Also shown are the GPS-45 battery indicator levels as measured at the internal battery connections. Voltage measured at the external power connector (when power is supplied externally) is about 0.5 volt higher. Power delivered to the load was integrated over time until the voltage reached 0.875 volts (the turn-off voltage) and the resulting energy expressed in W-Hrs is given below the curve label for each battery type. Only a single cell was measured in each case and the Renewal cell had been cycled about three times.*
>
> *H. Ward (hrward@ultranet.com)*

Which batteries are chosen depend greatly on the electrical characteristics of the components in the design. For instance, the 80L186EC-16 microprocessor requires a V_{CC} range of 3.0 to 5.5 volts. The 80L186EC-13 microprocessor, however, requires a V_{CC} range of 2.7 to 5.5 volts. It is probably unwise to select two series AA alkaline batteries with out any kind of power regulation as the power source for the 80L186EC-16 microprocessor. The chip would likely function for a very short period of time (less than one hour) before the voltage output of the batteries dropped below the operational threshold of the chip. However, the 13Mhz 80L186-13, which is probably a de-rated version of its 16Mhz counterpart, has a broader V_{CC} tolerance. This higher tolerance allows for a greater voltage drop before failure, which in turn leads to a longer (about 10 hours at 50mA with Energizer AA alkaline batteries) run time of the microprocessor. However, in both situations, the batteries still have significant service life remaining. Therefore, both solutions are poor designs.

Three series NiMH AA batteries will provide more than twice the current, 120mA, between 3.6 volts and 2.7 volts for almost eleven hours. The time can be doubled to almost 22 hours if we use six AA batteries by combining two serial stacks of three AA batteries in parallel. However, six AA batteries is a lot of batteries. This is an expensive solution for a high-use system unless rechargeable batteries are used.

Three series AA alkaline batteries will likely provide 100mA to 120mA at between 4.5 volts and 2.7 volts for approximately 20 hours. Alkaline batteries will provide greater system life but at a higher cost. The next step then is to consider using a power regulator.

C. SYSTEM POWER ANALYSIS

An analysis of the systems power must include the microprocessor operating frequency, system operating voltage, and current consumption of each device. The following sections describe these analyses.

1. Microprocessor Operating Frequency

The issues driving CPU Operating Frequency are (1) positional update frequency and (2) tactor drive signal switching speed. The PCNS must be capable of updating the user with new positional data at a minimum useful rate. This rate can be defined by the intended use of the system. Here we will make two assumptions. First, we will assume that the maximum ground speed at which the system will ever likely be used is 11 m/s (approximately 25 mph). Second, we will assume that the system will be used in conjunction with commercially available GPS receivers which have an accuracy of no more than 10 meters (30 feet). This means that the system will need to update the user at a rate just under once per second. In the absence of definitive human processing data, these assumptions provide some engineering bases for defining the requirements. As a result of these assumptions, the PCNS must be capable of updating the user at least 1.12 times each second or once every 895ms.

The second issue driving the operating frequency is the tactor drive signal switching frequency. The CPU must generate a switched signal with which to drive the tactors. The tactors require this signal to have a frequency of 250Hz. This is easily achievable with even slow processors. See Table 8. Tactor Update Execution Time by CPU Speed and Table 9. Calculation of Time Remaining for Useful Program Execution.

The CPU speed is, therefore, not a critical factor. The microprocessor can be expected to accomplish these jobs with an operating frequency of at least 8MHz. The operating frequency does, however, effect the power consumption of the device. The faster the operation, the greater the power consumption. Therefore, it is more desirable to select a slower speed processor over a higher speed processor.

2. System Operating Voltage, Vcc

The operating voltage also greatly effects the power consumption of the device. Lowering the device operating voltage from 5V to 3V greatly reduces current consumption. This in turn reduces the power consumption of the device because current consumption is directly

related to power consumption (P=IV). Battery life is also directly related to current consumption. Therefore, reduced voltage also leads to longer battery life with fewer batteries (i.e. less weight).

3. Microprocessor Power Consumption

The principle elements of the PNCC power consumption are the currents required by the (1) microprocessor, (2) the tactors, (3) the SRAM, and (4) the FLASH memory. The microprocessor current consumption (I_{CC}) is composed of the following two components.

(a) I_{PD} The quiescent current representing internal device leakage. Typically measured without a clock signal applied and with all inputs tied to either Vcc or to ground.

(b) I_{CCS} The current used to charge and discharge the devices internal parasitic capacitance while changing logic levels. This current is directly related to the frequency of operation, *f*, and the source voltage, Vcc. I_{CCS} is given by the following formula:

$$I_{CC} = C\frac{dV}{dt} \approx \Delta V \times C \times f$$

$$Power = V \times I = V^2 \times C_{PD} \times f$$

$$\therefore I_{CCS} = V_{CC} \times C_{PD} \times f$$

However, direct determination of the device capacitance, C_{PD}, is difficult. Therefore, the parameter is calculated with the above formula by measuring Icc, Vcc, and *f*. The calculated values for CPD are given below:

Table 1. Power Dissipation Capacitance for 80C186 Family [Ref 2].

Parameter	Typical	Max	Units
C_{PD}	0.77	1.37	mA/V*Mhz
C_{PD} (Idle Mode)	0.55	0.96	mA/V*Mhz

From these values, I_{CC} may be determined for any frequency and operating voltage. The Maximum "Worst Case" currents for two different microprocessors are compared below.

Icc for the Intel 80L186EC-13

Vcc = 3.0V

f = 13Mhz

C_{PD} = 1.37 mA/V*Mhz

Icc = 53.73mA

Icc for the Intel 80C186EC-25

Vcc = 5.0V

f = 25Mhz

C_{PD} = 1.37 mA/V*Mhz

Icc = 171.35mA

Icc Ratio

$$\frac{80L186EC-25}{80L186EC-13} \Rightarrow \frac{171.35mA}{53.7mA} \approx 3.2$$

Power Ratio

$$\frac{80L186EC-25}{80C186EC-13} \Rightarrow \frac{(5.0V)(171.4mA)}{(3.0V)(53.7mA)} = \frac{856.75mW}{161.2mW} \approx 5.3$$

From these calculations, it seems reasonable to expect that the 80L186-13 will last at least three times as long and will generate considerably less heat than the 80C186-25 under similar conditions. Similar worst case currents can be determined for all microprocessors

under consideration. In some cases, however, the vendor does not provide the C_{PD} for their chip. This number can generally be determined from the provided information. Table 2 compares the current requirements for various microprocessors that exhibit the desirable capabilities described in the section "CPU Selection."

Table 2. Comparison of Maximum Worst Case ICC Currents by Microprocessor.

Microprocessor	Operating Voltage	Icc	Current Ratio
Intel 80L186EC-13	3V	54 mA	1
Intel 80L186EC-16	3V	66 mA	1.2
Intel 80C186EC-25	5V	171 mA	3.2
Intel 80386EX-25	3V	140 mA	2.6
AMD186ED-40	5V	236 mA	4.4
AMD186EDLV-25	3V	100 mA	1.9

Example: Determining C_{PD} for AMD186EDLV-25

AMD provides the following information:

f = 25 MHz

V = V_{CC} = 3.0 V

I_{CC} = 100 mA (test data)

$$\therefore C_{PD} = \frac{I_{CC}}{V_{CC} \bullet f} = \frac{100mA}{(3.0v)(25MHz)} = 1.11\frac{mA}{V \bullet MHz}$$

The power analysis for the remaining devices can be found in the respective sections for that device. The PNCC Device List, which can be found in APPENDIX A – DEVICE LIST, contains a list of all parts in this design and their respective current consumption. John Williams details this type of analysis in his paper, *Low Voltage Embedded Design – Application Note 477*, [Ref 1].

When calculating the current consumption of a microprocessor base system, however, we need to consider one more current sink. The current consumed by the inputs and outputs switching. To determine this I/O current, we need to consider the voltage swing of the device

outputs, the input capacitance of the devices connected to the outputs, and the frequency of switching. The general formula for calculating the current **per pin** is:

$$I = C\int\frac{dV}{dt}$$

The pins that change most frequently during the normal operation of the CPU should be considered. For this design, the relevant pins are (1) the multiplexed address/data bus (A[19:16], AD[15:0]), (2) the address/data bus control lines ($\overline{RD}$, $\overline{WR}$, ALE), and (3) the tactor control lines (TC_[A:C], TC_[0:2]). Because the Intel 80L186EC uses a multiplexed address and data bus, we must consider the switching rates of the multiplexed bus for both the normal read and normal write operations independently. To determine the current consumption of the address/data bus during the write operation, I_{WRITE}, consider Figure 16. 80L186EC Typical 16-Bit Write Operation. The formula for I_{WRITE} then becomes:

$$I_{WRITE} = V \times C \times f \times \frac{(a+d)}{n}$$

Where:

V = Voltage swing of the pin, Vcc.
C = Input capacitance of the device to which the pin is connected (+2pF in of trace)
f = Frequency of operation (speed of the CPU)
n = Number of clock cycles per bus operation
a = Number of pins switching during the address phase
d = Number of pins switching during the data phase

V = Vcc = 3.3 volts. Since the microprocessor is connected to the Samsung KM616U4000C SRAM and a bank of three MC74LCX373 Low-Voltage Octal Latches, as described in the following sections, the input capacitance is 8pF and 7pF respectively, see Table 3. MC74LCX373 Dynamic Capacitance [Ref 9] and Table 14. KM616U4000 DC Operating Characteristics & Capacitance [Ref 15]. The frequency of switching, *f*, is the operating frequency

of the CPU. In our case 13Mhz. The final term, $\frac{(a+d)}{n}$, the number of pins switching per bus cycle, is somewhat more difficult to determine as it is highly dependent on the actual program that is implemented. However, because of the random nature of the data being read and written on the address/data bus, it is reasonable to assume that approximately half of the address/data pins will switch during each phase of the bus cycle. For the write operation, $a = \frac{16}{2}, d = \frac{16}{2}$. Therefore, the resulting current is

$$I_{WRITE} = (3.0V)(7pF)(13Mhz)\frac{(8+8)}{4} = 1.1mA.$$

Similarly, to calculate the current consumed during a read operation, I_{READ}, consider Figure 17. 80L186EC Typical 16-Bit Read Operation. In this case, d = 0 because the CPU does not drive the changing pins, I_{READ} then becomes

$$I_{READ} = (3.0V)(7pF)(13Mhz)\frac{(8+0)}{4} = 0.55mA$$

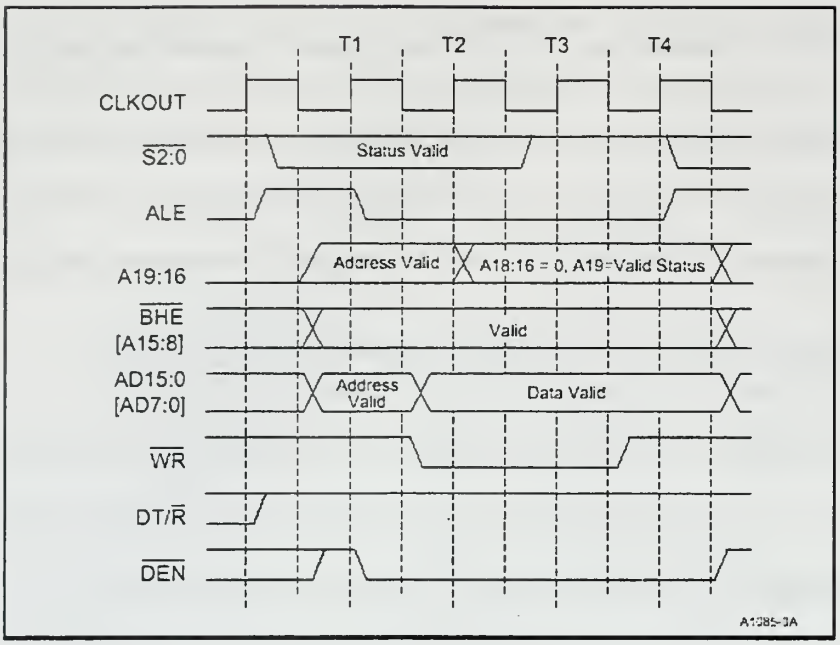


Figure 16. 80L186EC Typical 16-Bit Write Operation [Ref 2].

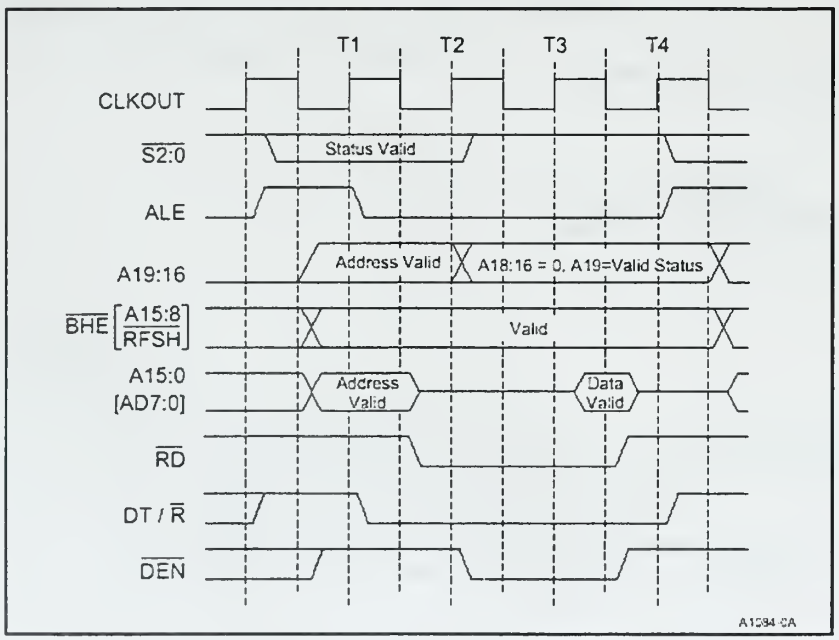


Figure 17. 80L186EC Typical 16-Bit Read Operation [Ref 2].

Table 3. MC74LCX373 Dynamic Capacitance [Ref 9].

Symbol	Characteristic	Condition	TA = +25°C			
			Min	Typ	Max	Unit
VOLP	Dynamic LOW Peak Voltage (Note 4.)	VCC = 3.3V, CL = 50pF, VIH = 3.3V, VIL = 0V		0.8		V
VOLV	Dynamic LOW Valley Voltage (Note 4.)	VCC = 3.3V, CL = 50pF, VIH = 3.3V, VIL = 0V		0.8		V

To determine the current resulting from the switching of the control lines, $I_{CONTROL}$, we need to consider the number of times the control lines, specifically $\overline{RD}, \overline{WR}, ALE$, switch during the read and write operations. From the previous figures, we see that they each switch twice during both the read and write operations. Therefore,

$$I_{CONTROL} = (3.0V)(7\,pF)(13Mhz)\frac{(2+2+2)}{4} = 0.41mA$$

The current consumed by switching the tactor control lines, I_{TCTRL}, will be three orders of magnitude lower than $I_{CONTROL}$, I_{READ}, and I_{WRITE} due to the frequency of switching (i.e. 250Hz versus 13Mhz). Therefore, we will ignore I_{TCTRL}. The total IO current for the 80L186EC is then the sum of the three currents, $I_{CONTROL}$, I_{READ}, and I_{WRITE}. However, we must take into account the relative number of reads and writes performed during the execution of the program. Previous analyses of program executions have demonstrated that a reasonable assumption is 80% of bus operations are reads while 20% are writes [Ref 1]. The total IO current is then,

$$I_{IO} = I_{CONTROL} + (0.8)I_{READ} + (0.2)I_{WRITE} = 0.44mA + (0.8)(0.55mA) + (0.2)(1.1mA) = 1.1mA$$

The IO current is very small in comparison to the worst case Icc for the 80L186EC-13 and as such can be ignored. A similar analysis could be performed for every other component in the system.

D. Power Supply Implementation Overview

The power supply consists primarily of three elements, (1) a battery pack, (2) a voltage regulator, and (3) a microprocessor monitor. The voltage regulator and microprocessor monitor are discussed in detail in the following section. The battery pack has already been addressed above.

The user has three inputs to the power supply. These inputs are (1) the on/off switch, (2) a manual "hard" reset, and (3) a power on test button. The on/off switch controls the primary input power to the entire system. The manual reset button causes the active low RESIN pin of the microprocessor to be driven low. The power on test button will momentarily illuminate a LED if power is delivered to the system via the batteries and the on/off switch.

The power on test button is a normally open momentary contact with two purposes. First, it provides a mechanism by which the user can directly determine if the system is turned on. Second, it reduces current consumption of the system by only illuminating a LED while the user cares to determine the systems "power on" status.

The purpose of the manual reset button is to provide a direct mechanism for the user to reset the system. This hard reset button is a normally open momentary contact switch which is tied across the $\overline{MR}$ and GND pins of the MAXIM MAX6319LH microprocessor supervisor. When the button is depressed the $\overline{MR}$ pin of the supervisor is driven low which causes the supervisor to drive its $\overline{RESET}$ output pin low. This $\overline{RESET}$ pin is in turn connected to the microprocessor's $\overline{RESIN}$ pin which causes a hard reset of the microprocessor. The supervisor provides an additional service to the system. It also monitors V_{CC}. If the output of the voltage regulator falls below the threshold voltage of 2.7 volts, ±0.04V at 25C, the supervisor will drive its $\overline{RESIN}$ pin low and hold it low until the voltage rises above 2.7 volts. The supervisor is capabable of performing this function as long as its V_{CC} voltage is at least 1.0 volts. No external debouncing circuitry is required. A 100KΩ resistor is tied between V_{CC} and the $\overline{MR}$ input to drive the pin high. However, a 52KΩ internal pull-up resistor is present in the device and the 100KΩ resistor is extra protection. A 0.1uF capacitor is tied between the $\overline{MR}$ input and gound

to provide additional noise immunity to the supervisor. This supervisor chip was selected to have a 30ms (±10ms) nominal undervoltage wait duration before it would assert the RESET signal. This selection was arbitrary.

The on/off switch is a SPST switch connected to the MAXIM MAX6817 Dual Switch Debouncer between it's IN1 and ground pins. The IN1 pin is also connected to V_{CC} through a 1MΩ resistor. The state of the switch debouncers OUT1 pin is a debounced version of the voltage on the IN1 pin. The OUT1 pin is subsequently wired to the $\overline{OFF}$ pin of the MAXIM MAX603 voltage regulator. The power regulator is described in detail in the following section.

E. Power Regulation

The job of the power supply is to (1) provide a constant stable voltage and (2) accommodate the current demands of the circuit. One solution is to simply strap the battery output terminal directly into the circuit. This solution is adequate if the circuit components are tolerant of voltage variances. For instance, the Intel 80C186EC-13 microprocessor can operate with a V_{CC} range of 2.7 to 5.5 volts. However, the Samsung KM616U4000C Static RAM can only operate with a VCC range of 2.7 to 3.3 volts. Sometimes the chips may function at a given voltage level but will operate more efficiently at a different level. An example of this is the Transparent Octal Latch by Motorola. The MC74LCX373 will draw 12mA when driven with a V_{CC} between 2.7 and 3.0 volts. However, it draws 24mA when driven with a V_{CC} higher than 3.0 volts. Therefore, careful analysis of the power requirements of every circuit component is required before a decision can be made about whether or not to use power regulation.

The disadvantage to using a power regulator is, of course, additional current consumption, form factor (size & weight), cost, circuit complexity, and heat. For this design the primary concern is power consumption. The return on investment analysis of the power regulator provides a convincing argument for the use of a regulator. As described earlier, our design will most likely use either three alkaline or three rechargeable AA batteries as its power source. This means that the input voltage of the system will either vary from 4.5 to 2.7 volts, in the case of

alkaline batteries, or vary from 3.6 to 2.7 volts, in the case of rechargeable batteries. In either case, the voltage level will at some time be greater than maximum recommended operating voltage for at least one component. APPENDIX A – DEVICE LIST provides a comprehensive listing of operating voltage requirements and current consumption for each component in this design.

1. The MAXIM MAX603 Power Regulator

The MAX603 and MAX604 are low-quiescent current, low dropout linear voltage regulators. They can supply an adjustable 1.25 to 11 volt output or a fixed 3.3 volt or 5 volt output. They can supply these voltage levels for any current output up to 500mA. The MAX603/MAX604 features an internal P-Channel pass transistor that limits the regulators quiescent current to approximately 15μA under light and heavy loads. Because the MOSFET requires no base drive, it reduces the regulators quiescent current considerably.

The MAX603/MAX604 have two other features of interest. They support a shutdown feature and reverse-current protection. Driving the $\overline{OFF}$ pin to ground may drive this regulator into a shutdown mode. In this mode, the regulator turns off the pass transistor, control circuit, reference, and all biases. This reduces the supply current to less than 2μA and effectively kills all power to the PNCS.

The second feature of interest is the reverse-current protection. The regulator monitors the output and input voltages. If V_{IN} falls below V_{OUT} it switches the IC's substrate and power bus to the more positive of the two. This allows the control circuitry to continue functioning and turn the pass transistor off. This feature activates when V_{IN} falls 6mV below V_{OUT}.

2. Power Regulator Integration

The output voltage of the regulator is either fixed or can be manually set by selecting the appropriate resistors for R_1 and R_2. See the power circuit schematic in APPENDIX B – CIRCUIT SCHEMATICS. If the input to V_{SET} is grounded then the output of the regulator is either 3.30 volts or 5.00 volts depending on the model, MAX603 and MAX604 respectively. However, if, as in our

case, a different output voltage is desired, then adding a resistor network to the input of V_{SET} will customize the output voltage. The governing equations for R_1 and R_2 are:

$$V_{OUT} = V_{SET}\left(1 + \frac{R_1}{R_2}\right)$$

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{SET}} - 1\right)$$

where V_{SET} = 1.20 Volts.

For our design we want the output voltage to be 3.00 volts.

$$\therefore R_1 = R_2\left(\frac{3.00Volts}{1.20Volts} - 1\right) = 1.50R_2$$

The input bias current at V_{SET} is nominally zero. Therefore, large resistance values may be used for R1 and R2 to minimize power consumption without losing accuracy. According to the data sheet, values up to 1.5MΩ are acceptable for R_2. The voltage tolerance at V_{SET} is less than ± 40mV. For the prototype design a trim pot should be used to adjust the output voltage. However, the V_{SET} tolerance is low enough that a resistor network of 1% accuracy resistors should be adequate for establishing the proper output voltage.

The actual value of the resistors in the resistor network can have a significant effect on the regulators actual output voltage. Table 4 below shows the possible ranges of outputs given various resistor tolerances assuming $R_1 = 1.50R_2$ and R_2 = 100KΩ.

Table 4. Effect of Resistor Tolerance on Regulated Output Voltage.

Resistor Tolerance	VOUT	
	Maximum (volts)	Minimum (volts)
1%	3.04	2.96
2%	3.07	2.93
5%	3.19	2.83
10%	3.4	2.67
20%	3.9	2.4

The selection of capacitors for the MAX603 is based on regulator stability or noise rejection capability. The Maxim data sheet recommends capacitors in the range of 0.1μF to 10μF. For greater noise rejection, use larger capacitors. The supply side of the regulator is battery powered. Batteries are typically very stable and not noisy. A smaller capacitor such as a 3.3μF capacitor should be used. The output side of the regulator is likely to be very noisy, based on the nature of a clocked digital device. Therefore, a 10μF capacitor should be used.

V. THE MICROPROCESSOR

A. SELECTING AN EMBEDDED PLATFORM

The most significant constraint for selecting the embedded platform for this design is power. If we consider the intended use of the device, that being land navigation using global positioning system inputs, then we must accept that this system is intended for extended, continuous, and portable use. This implies that the system must necessarily be light weight, small, and battery powered. It is also very likely that the system will be needed for several hours of continuous operation. For instance, campers and hikers may want the system to function continuously for several hours a day for an entire weekend or possibly a week long vacation. As a result, the final design should be capable of running continuously for many (at least 8) hours on only a few (two to six) small (AA) batteries.

Therefore, the embedded processor selection criteria are defined to be the following:

1. Low Power Consumption (small I_{CC})
2. Lower Operating Frequency (current consumption is directly proportional to operating frequency)
3. CPU/Peripheral Integration (reduced heat, size, weight, and current consumption)
4. Adequate Memory Space (at least 1MB of addressable space)
5. At least two integrated serial I/O communications controllers (GPS and either a Laptop/Diagnostic or digital radio)
6. Well established chip manufacture and vendors (reliability)

A great many chips were initially investigated. However, the final selection came down to one of (1) the AMD186EDLV, (2) the Motorola M86HC916, (3) the Intel 80386EX, (4) or the Intel 80L186EC.

B. OVERVIEW OF THE INTEL 80L186EC

The 80L186EC is the low voltage variant of the 80C186EC and belongs to the Intel 80C186 family of microprocessors. This family consists of the 80C186EX, 80C186EA, 80C186EB, and the 80C186EC. The EC is the most integrated member of the family. The EC provides two full featured serial ports, four DMA channels, a flexible chip select unit, three general

purpose timer/counters, a watchdog timer, two 8259A interrupt controllers, a DRAM refresh control unit, and 24 multiplexed I/O pins. Table 5 shows the relative levels of integration within the 80C186 family [Ref 10].

Table 5. Comparison of 80C186 Family Integrated Peripherials.

Feature	80C186XL	80C186EA	80C186EB	80C186EC
Enhanced 8086 Instruction Set				
Low-Power Static Modular CPU				
Power-Save (Clock Divide) Mode				
Powerdown and Idle Mode				
80C187 Interface				
ONCE Mode				
Interrupt Control Unit				8259 Compatible
Timer/Counter Unit				
Chip-Select Unit			Enhanced	Enhanced
DMA Unit	2 Channel	2 Channel		4 Channel
Serial Communications Unit				
DRAM Refresh Control Unit			Enhanced	Enhanced
Watchdog Timer Unit				
I/O Ports			16 Total	22 Total

The 80L186EC is designed to provide low power operation by utilizing a 3V operating voltage, integrated peripherals, and a power down mode that halts the clock. Non-initialized peripherals consume little current. A detailed analysis of the power consumption and operating frequency of this device is provided in the previous section on the power system. Figure 18. 80L186EC Simplified Functional Block Diagram is obtained from reference 11.

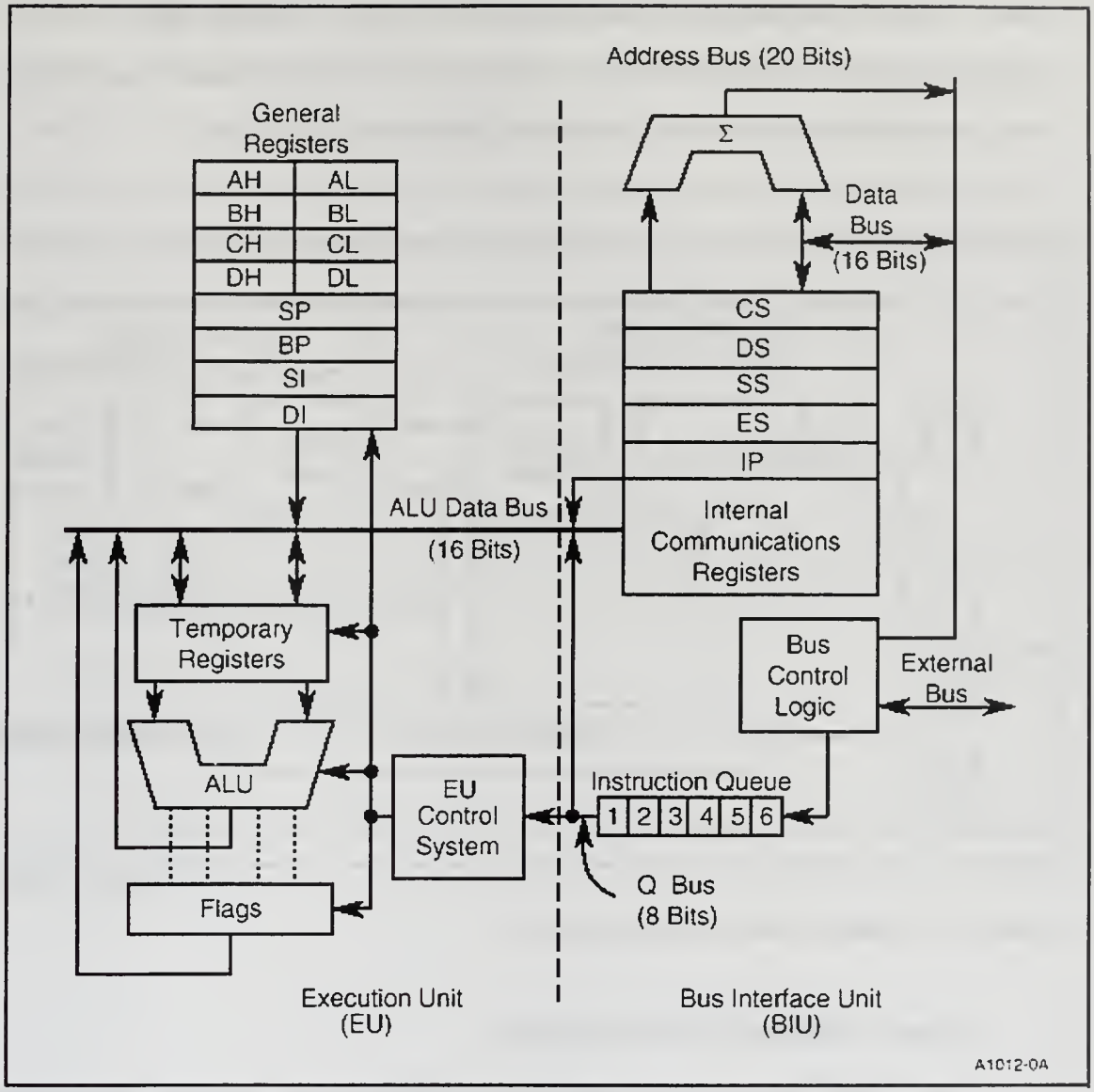


Figure 18. 80L186EC Simplified Functional Block Diagram [Ref 11].

C. CLOCKING

Either a crystal oscillator or an external oscillator can drive this microprocessor. A crystal is typically less expensive and will consume less power than an external oscillator. Therefore, this design will employ a crystal oscillator. The company ILSI makes a 2mm x 6mm crystal oscillator with a parallel resonant frequency of 26.000000 MHz. This crystal is a fundamental overtone oscillator with a maximum Equivalent Series Resistance (ESR) of 60 ohms. The part number for this crystal is 26 260-30. See Appendix E for the more technical data regarding this

crystal. This microprocessor uses an internal divide by 2 counter. Therefore, using a 26 MHz crystal will generate a 13MHz clock frequency. Figure 19. 80L186EC Clock Generation Circuit below depicts the internal construction of the clock generation circuit [Ref 11].

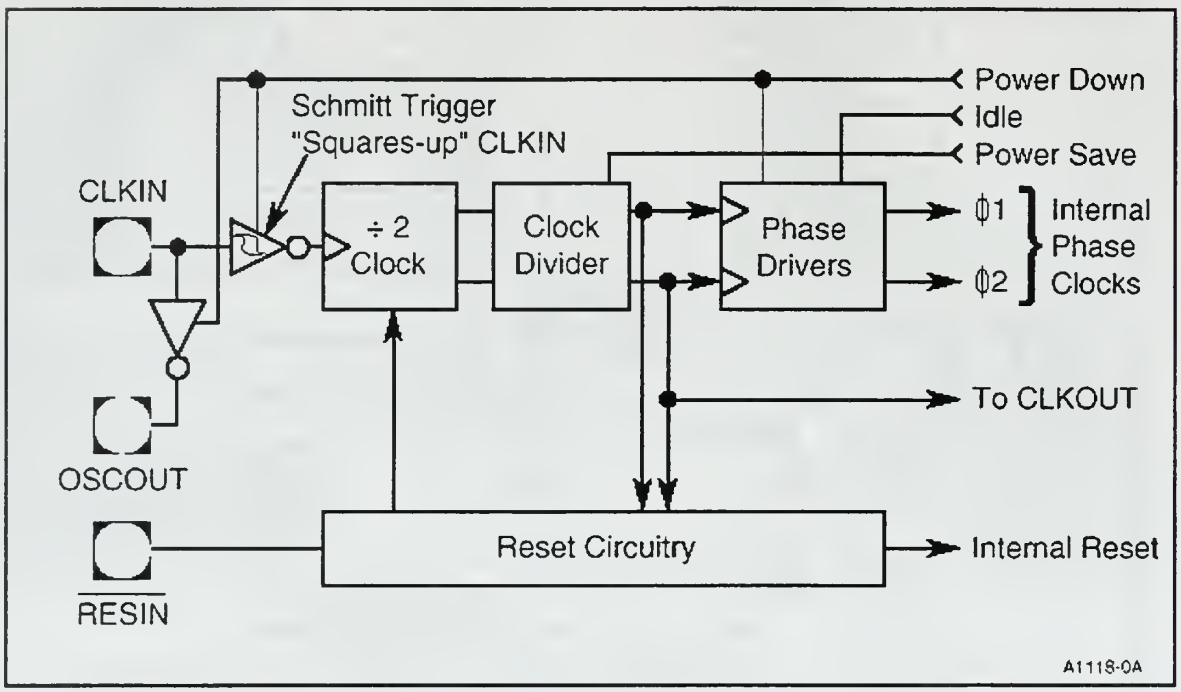


Figure 19. 80L186EC Clock Generation Circuit.

D. SERIAL COMMUNICATIONS INTERFACE

The 80L186EC has two internal serial communications ports or channels. Each channel is completely independent of the other channel and is fully configurable. The serial channels support the following features:

1. Full duplex operation
2. Programmable seven, eight or nine data bits in asynchronous mode
3. Independent baud rate generators
4. Maximum baud rate of 1/16 the processor clock
5. Double-buffered transmit and receive
6. Clear-to-Send feature for transmission
7. Break character transmission and detection
8. Programmable even, odd or no parity
9. Detects both framing and overrun errors
10. Supports interrupt on transmit and receive

These serial ports can be used to support the communications link for both the GPS receiver and a diagnostic computer. Pre-loading certain control registers with the proper bits configures the serial ports on the 80L186EC. The proper control values will need to be determined by the user depending on the communication requirements of the selected GPS receiver and diagnostic computer. Figure 20 below, shows the structure of the 80L186EC serial port communications when it is configured for 7 data bits embedded in one start bit and one stop bit with parity.

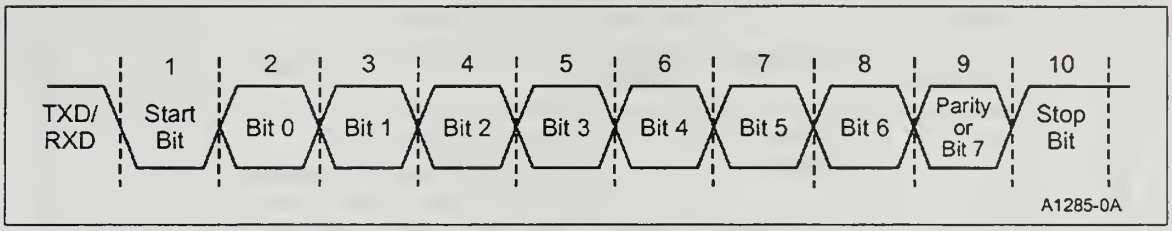


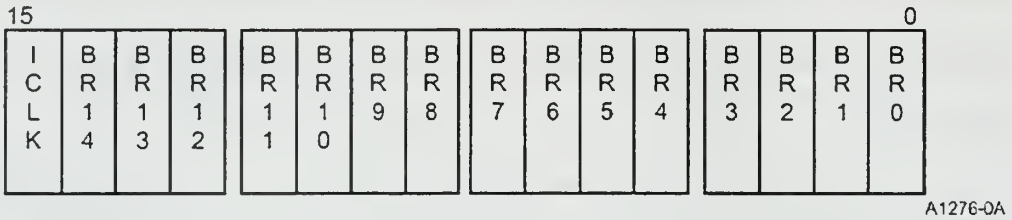
Figure 20. 80L186EC: 7-Bit with Parity Serial Waveform [Ref 11].

The following tables depict the Baud Rate Compare Register and the Serial Port Control Register [Ref 11].

Register Name: Baud Rate Compare Register

Register Mnemonic: BxCMP

Register Function: Determines baud rate for the serial port.



Bit Mnemonic	Bit Name	Reset State	Function
ICLK	Internal Clocking	0	Selects the input clock: 0 = BCLK is input to baud clock. 1 = CPU clock is input to baud clock.
BR14:0	Baud Rate Compare Field	0	Sets the compare value for the baud rate clock.

Figure 21. 80L186EC Baud Rate Compare Register [Ref 11].

The Baud Rate Compare Register is used to program the baud rate of the serial port. Each serial port on the 80L186EC is independently configurable. Thus there are two different Baud Rate Compare Registers in the 80L186EC. These registers are programmed with a count value that then determines the baud rate of the respective serial port. Obviously, the clock rate of the CPU will directly affect the baud rate. The following figure provides some typical values used to arrive at commonly used baud rates.

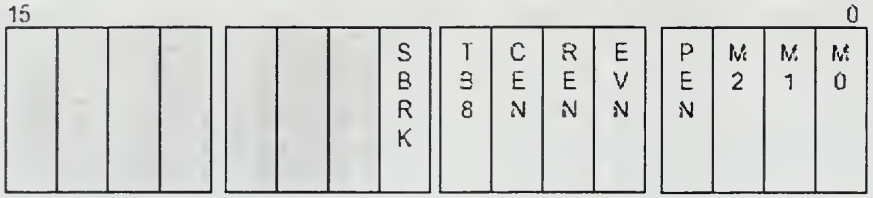
Baud Rate	CPU Frequency							
	25 MHz		20 MHz		16 MHz		8 MHz	
	BxCMP Value	% Error	BxCMP Value	% Error	BxCMP Value	% Error	BxCMP Value	% Error
19,200	80A2H	–0.14	8081H	0.16	8067H	0.16	8033H	0.16
9,600	8145H	–0.14	8103H	0.16	80CFH	0.16	8067H	0.16
4,800	828AH	0.00	8208H	–0.03	81A0H	–0.08	80CFH	0.16
2,400	8515H	0.00	8411H	–0.03	8340H	0.04	81A0H	–0.08
1,200	8A2BH	0.00	8822H	0.01	8682H	–0.02	8340H	0.04

Figure 22. Typical Baud Rate Compare Values for the 80L186EC [Ref 11].

Register Name: Serial Port Control Register

Register Mnemonic: SxCON

Register Function: Controls serial port operating modes.



A1277-0A

Bit Mnemonic	Bit Name	Reset State	Function
SBRK	Send Break	0	Setting SBRK drives TXD low. TXD remains low until SBRK is cleared.
TB8	Transmitted Bit 8	0	TB8 is the eighth data bit transmitted in modes 2 and 3.
CEN	Clear-to-Send Enable	0	When CEN is set, no transmissions will occur until the $\overline{CTS}$ pin is asserted.
REN	Receive Enable	0	Set to enable the receive machine.
EVN	Even Parity Select	0	When parity is enabled, EVN selects between even and odd parity. Set for even, clear for odd parity.
PEN	Parity Enable	0	Setting PEN enables the parity generation/checking for all transmissions/receptions.
M2:0	Serial Port Mode Field	0	Operating mode for the serial port channel. **M2 M1 M0 Mode** 0 0 0 Synchronous Mode0 0 0 1 10-Bit Asynch Mode1 0 1 0 11-Bit Asynch Mode2 0 1 1 11-Bit Asynch Mode3 1 0 0 9-Bit Asynch Mode4 1 0 1 Reserved 1 1 0 Reserved 1 1 1 Reserved

NOTE: Reserved register bits are shown with gray shading. Reserved bits must be written to a logic zero to ensure compatibility with future Intel products.

Figure 23. 80L186EC Serial Port Control Register [Ref 11].

The configuration of the communications ports is fundamental to the operation of the PNCS as a system. Therefore, these ports should be configured automatically during the startup sequence of the system. The 80L186EC clearly has the capability to interface with a wide variety of serial communication equipped peripheral equipment regardless of the limitations of the peripherals.

E. PERFORMANCE

1. PNCS Timing Requirements Definition

The ability of the microprocessor to meet the minimum timing requirements of the system must also be taken into account. The following is a list of the timing requirements the PNCS imposes on its CPU. These requirements are derived from the requirements defined at the beginning of this thesis. The CPU must:

1. Generate a 250 Hz power signal to drive up to eight tactors.
2. Receive & decode messages from an external GPS receiver at least once per second.
3. Control (i.e. turn on or off) up to eight tactors at least 2 times each per second.

The need for the first requirement is driven by the technical requirements of the tactors. See APPENDIX F – TECHNICAL DATA SHEETS for more technical details regarding the tactors. The second requirement is less technically driven. The PNCS must be capable of updating the user frequently enough that the principle objective of the system is still accomplished. That objective is for the PNCS to function as a terrestrial navigation tool for pedestrians. As such, the PNCS must be capable of updating the user frequently enough that the user does not get too far off course in between updates. The traveling velocity of a pedestrian is not significantly high that a very high update rate is required. The last requirement is driven by the need to pulse one or more tactor(s) for communication with the user.

2. 80L186EC Timing Performance

In order for the 80L186EC to meet the first timing requirement, generation of the 250 Hz signal, it must be capable of executing code fast enough to toggle up to six of its programmable I/O pins at a rate of at least 250 Hz. The CPU will control the eight tactors by generating individual power signals for each tactor. These power signals are controlled by six logic level outputs on the 80L186EC (see the section on the tactor Interface for more details regarding how the CPU controls eight tactors with six control lines). The CPU needs to generate a "tactor

control word" (TCW – six bits in length) that is updated every 4ms. Therefore, the CPU must have a clock speed sufficient to execute a simple program capable of changing the TCW within 4mS. This is easily achievable for a CPU running at 13MHz. Table 6 provides a crude estimation of program execution times for an 80L186EC CPU running at 8MHz, 16MHz, 20MHz, or 25MHz. This table lists the length of time the CPU would take if it were to execute a program containing 1000 instruction assuming an average of 20 clocks are required to execute each instruction [Ref 2]. This is not a very accurate way of estimating execution time, however, short of having the actual program code, this does provide some general rough order of magnitude timing information.

Table 6. 80L186EC Program Execution Time.

CPU Speed (MHz)	8	13	16	20	25
Clock Period (ns)	125.0	76.9	62.5	50.0	40.0
Average Clocks Per Instruction	20.0	20.0	20.0	20.0	20.0
Average Time Per Instruction (ns)	2500.0	1538.5	1250.0	1000.0	800.0
Average Instructions Per Program	1000.0	1000.0	1000.0	1000.0	1000.0
Average Time Per Program (ms)	2.5	1.5	1.3	1.0	0.8

Since the actual program will consist of something like an interrupt service routine that simply performs a couple of memory operations, a logical comparison or two, and then changes the state of up to six programmable I/O pins, the actual program will require more like 21μs to 66μs. See Table 7. Program Execution Time Calculation for Hypothetical Tactor Update Program and Table 8. Tactor Update Execution Time by CPU Speed below. The data for these tables comes from the *80C186EC/180C188EC and 80L186EC/80L188EC 16-Bit High Integration Embedded Processors - Data Sheet*, [Ref 11].

Table 7. Program Execution Time Calculation for Hypothetical Tactor Update Program.

Instruction Type	Avg Clocks	Number of Instructions	Total Clocks
ISR	48	1	48
Memory	12	20	240
Logical	10	10	100
Set IO (Memory)	12	12	144
Total			**532**

Table 8. Tactor Update Execution Time by CPU Speed.

	CPU Speed (MHz)				
	8	**13**	**16**	**20**	**25**
Execution Time (uS)	66.50	40.92	33.25	26.60	21.28

The calculations in these tables are hypothetical because the actual source code for the program has not been defined and is beyond the scope of this thesis. However, these calculations serve as a reasonably good estimate of how much time the program might require. Based on these calculations, it is easy to see that this microprocessor will have no trouble meeting the timing requirements for driving the tactors at a 250 Hz rate and still have time to execute a productive program even if we assume the program length is off by as much as 100% to 200%. See Table 9 below.

Table 9. Calculation of Time Remaining for Useful Program Execution.

Update Requirement	1	sec
ISR Duration (Worst Case)	0.0001	sec
Number of ISR per Requirements	250	
ISR Time Required	0.025	sec
Time Remaining	0.975	sec

A similar analysis could be performed to generate a hypothetical execution time for communicating with the GPS and resolving the information into commands for the tactors. However, lets consider the problem from the other side. Instead lets calculate the maximum length of the program in instructions based on the maximum amount of time remaining. For a

very crude (and conservative) analysis, assume the average instruction length is 25 clocks. Then we could execute

$$\frac{1\ Instruction}{25\ Clocks} \times \frac{8 \times 10^6\ Clocks}{1\ Sec} \times 0.975\ Sec = 312000\ Instructions$$

The more likely bottleneck is not the speed of the CPU but rather the speed of the serial communications link between the CPU and the GPS. It is very probable that this link is limited by at most 9600 baud. For the following analysis we will assume the PNCS is communicating with a Garmin™ brand GPS using the Garmin™ Basic Link Protocol (BLP). See the *GARMIN GPS Interface Specification* [Ref 12] for more information on the Garmin™ interface specification. The Garmin™ BLP uses an EIA-232 serial communications specification operating at 9600 baud with 8 data bits, no parity, and 1 stop bit in full duplex mode. This means that the total length of one 8 bit data packet is 10 bits long, thus there is a 20% overhead on all communications at 9600 baud (assuming no errors). The Garmin™ BLP uses a six-byte overhead structure to package useful data into packets of variable byte length. The average length of a positional update package from the Garmin™ GPS is conservatively 80 bytes (74 data bytes + 3 header bytes + 3 trailer bytes) in length on average (depending on the model and mode of communication). Therefor, the number of positional updates that can be transmitted in 1 second are:

$$\frac{9600\ Bits}{Sec} \times 0.80 \times \frac{1\ Byte}{8\ Bits} \times \frac{1\ Message}{80\ Bytes} = 12\ Messages$$

The time to transmit 80 bytes over a 9600-baud transmission line with 20% overhead is 83.3ms. This does not take into account the BLP overhead associated with acknowledgments or clashes. However, there is clearly enough time to transmit enough packages to meet the final time requirement. The processing speed of the CPU is also adequate to execute a very long

program in the remaining 0.975 – 0.0833 = 0.891 seconds to interpret the data and generate the proper update word for the tactors.

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VI. MEMORY SYSTEM DESIGN

A. OVERVIEW

The system requirements as well as some design considerations drive the memory and operating system selections. Figure 24 shows a typical memory system for an Intel based embedded processor capable of using Microsoft DOS or Windows as its native operating system.

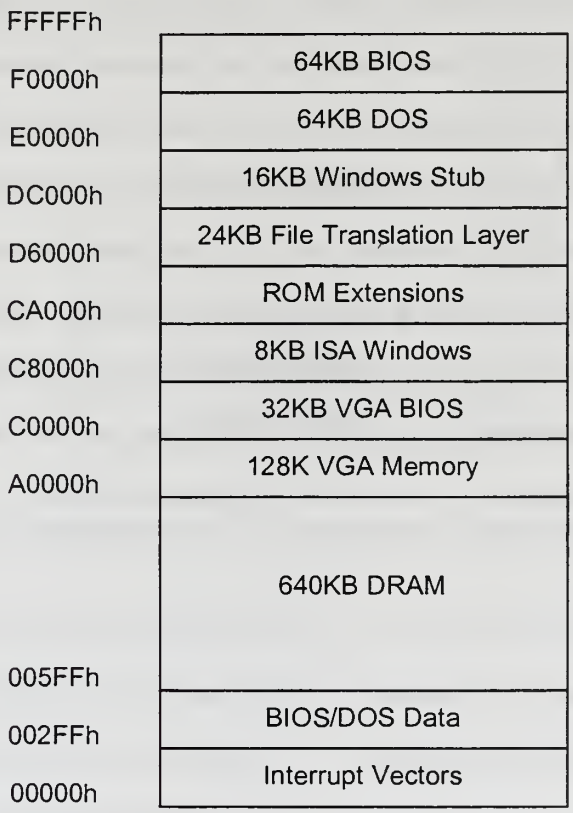

Figure 24. Typical Intel Processor Memory Map.

The memory system of the PNCC will not need to support all of the features of a regular desktop type of computer. For example, the PNCC will not support a floppy drive, hard disk drive, CD-ROM drive, keyboard, monitor, video system, sound cards, etc. It will also not need to access more than 1MB of address space. As a result, much of the address space allocated to

supporting these features may be used by the PNCC for other purposes. However, it is possible that a small LCD and keyboard may become desirable as a future expansion.

Generally, three kinds of memory hardware are considered for embedded system designs. PROM chips are used to house the BIOS and the OS. For the prototype designs an EEPROM or a UVPROM are used to simplify the implementation process and reduce costs associated with mistakes. FLASH memory is generally used to house the application code. Finally, RAM is used to provide scratch pad space for the BIOS, OS, and application program. This RAM is usually either SRAM or DRAM. The job of the memory system for the PNCC, then, is to (1) store the BIOS, Operating System, and the application program and (2) to provide scratch pad space for these programs. The PNCC memory subsystem will use two kinds of memory hardware. It will use FLASH memory to provide the non-volatile storage space for the BIOS, OS, and the application program; and, it will use SRAM to provide the scratch pad space.

Figure 25 below, details the memory map for the PNCC. This memory design was chosen to provide compatibility with existing BIOS and operating system products to simplify fabrication and programming of the computer. Using third party BOIS and operating systems also improves system reliability and reduces system development costs.

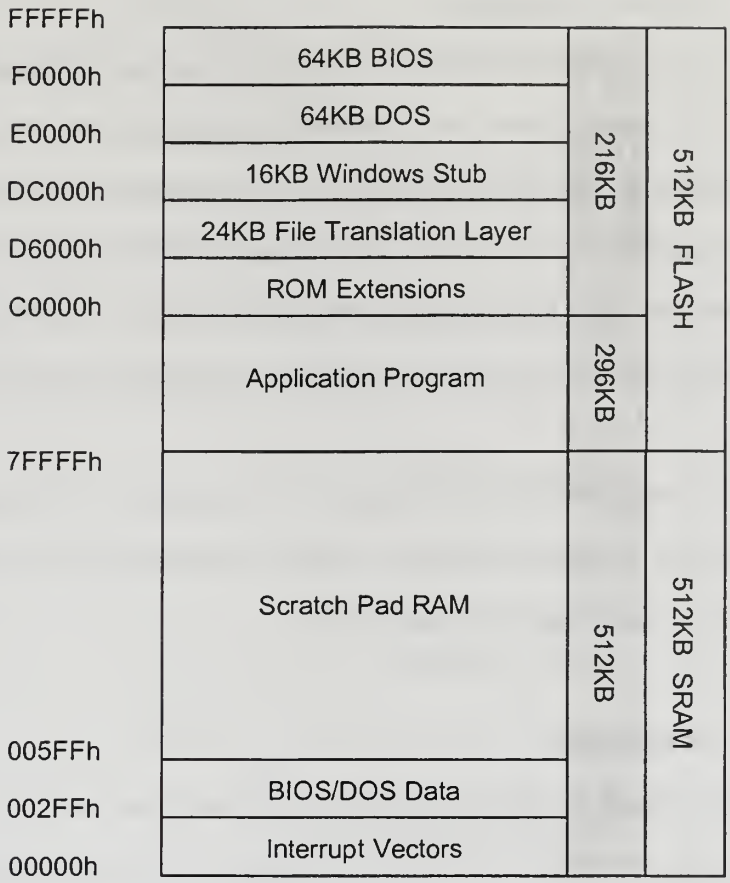

Figure 25. Personal Navigation and Communication Computer Memory Map.

A FLASH RAM and an SRAM chip were chosen to comprise the memory subsystem. The criteria used for selecting the chips were, in order of importance, (1) function, (2) size (address space), (3) low power (V_{CC} = 3V, lowest I_{CC}), (4) timing, (5) availability (must still be supported by the manufacturer), and (6) cost.

B. FLASH RAM

The FLASH RAM is responsible for the non-volatile storage of the BIOS, Operating System, and the application program. In addition, using a FLASH chip in this way allows us to design rapid upgrade capability into the PNCC. The drawback is that we now need to pay more careful attention to the write protecting features of the chip to prevent accidental code loss.

1. FLASH Fundamentals

Flash memory is similar to EEPROM. Like RAM, it can be electrically modified, however, like ROM it is a non-volatile medium and it will retain stored information even while powered down. Unlike RAM and ROM, however, the bytes of a flash may only be written if they are being written from an erase state to a non-erase state. During a "write" operation the bits of a flash byte are modified from their erase state to a non-erase state. During the "erase" process, all bits of the byte are returned to their erase state. A flash memory must be erased before it can be re-written.

Generally, entire blocks of flash are erased simultaneously. The manufacturer usually predefines the blocks. One erase operation is called a cycle. Cycles are sometimes used to determine the lifetime potential of the flash [Ref 13].

2. MT28F400B3

The MT28F400B3 FLASH RAM by Micron Technology, Inc. is a nonvolatile, electrically block-erasable (flash), programmable read-only memory containing 4,194,304 bits organized as 262,144 (256K) 16-bit words or 524,288 (512K) 8-bit words. Writing or erasing the device is done with a 3.3V (Vpp) voltage. All normal operations are performed with a 3.3V Vcc.

The FLASH RAM provides non-volatile storage space for the BIOS, OS, and the application program. The Micron MT28F400B3 has a hardware protected boot block. Figure 26 shows the memory organization of the chip. Figure 27 shows the functional block diagram of the device.

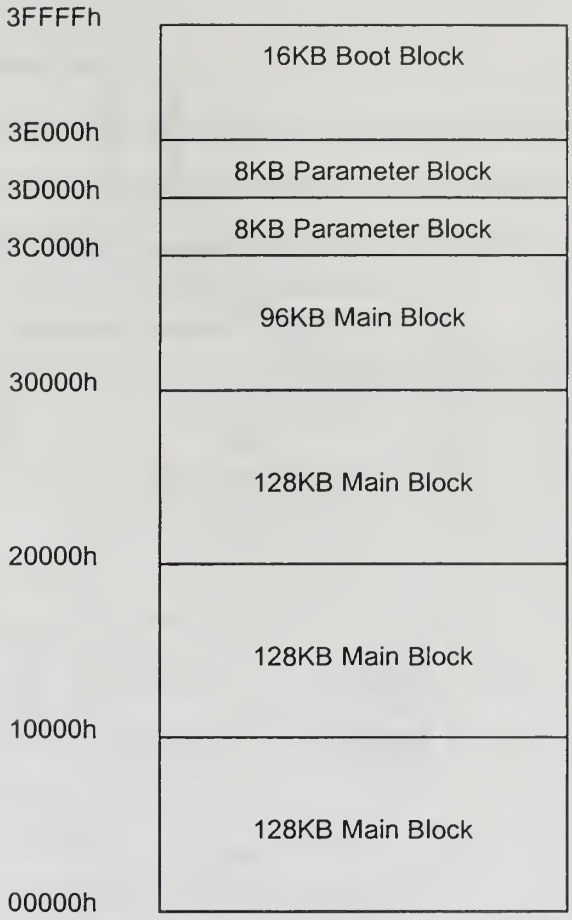

Figure 26. Memory Map of the MT28F400B3xx-xxT.

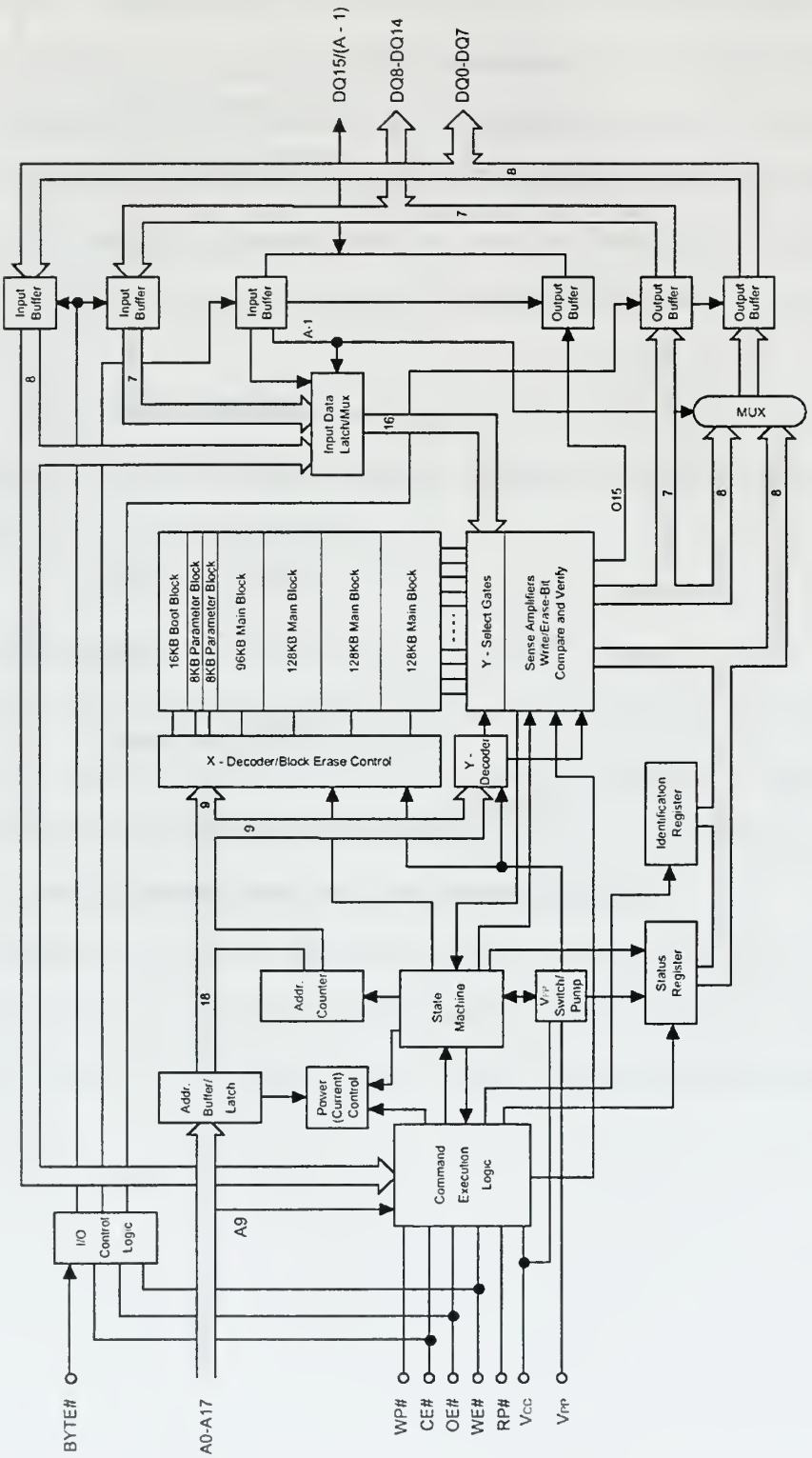

Figure 27. MT28F400B3 Functional Block Diagram [Ref 14].

3. Power Consumption

The power consumption of the FLASH device is, like the microprocessor, dependent on the internal design and the external pin switching. However, the manufacturer has provided us with this information, see Table 10 and Table 11 below.

Table 10. MT28F400B3 DC Operating Characteristics [Ref 14].

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
OUTPUT VOLTAGE LEVELS Output High Voltage (I_{OH} = -100µA) Output Low Voltage (I_{OL} = 2mA)	V_{OH} V_{OL}	2.4 –	– 0.45	V V	1
INPUT LEAKAGE CURRENT Any input (0V ≤ V_{IN} ≤ V_{CC}); All other pins not under test = 0V	I_L	-1	1	µA	
INPUT LEAKAGE CURRENT: A9 INPUT (11.4V ≤ A9 ≤ 12.6 = V_{ID})	I_{ID}	–	500	µA	
INPUT LEAKAGE CURRENT: RP# INPUT (11.4V ≤ RP# ≤ 12.6 = V_{HH})	I_{HH}	–	500	µA	
OUTPUT LEAKAGE CURRENT (D_{OUT} is disabled; 0V ≤ V_{OUT} ≤ V_{CC})	I_{OZ}	-10	10	µA	

NOTE: 1. All voltages referenced to V_{SS}.

Table 11. MT28F400B3 Read & Standby Current Drain [Ref 14].

PARAMETER/CONDITION	SYMBOL	MAX	UNITS	NOTES
READ CURRENT: WORD-WIDE, CMOS INPUT LEVELS (CE# ≤ 0.2V; OE# ≥ V_{CC} - 0.2V; f = 10 MHz; Other inputs ≤ 0.2V or ≥ V_{CC} - 0.2V; RP# ≥ V_{CC} - 0.2V)	I_{CC1}	15	mA	1, 2
READ CURRENT: BYTE-WIDE, CMOS INPUT LEVELS (CE# ≤ 0.2V; OE# ≥ V_{CC} - 0.2V; f = 10 MHz; Other inputs ≤ 0.2V or ≥ V_{CC} - 0.2V; RP# = V_{CC} - 0.2V)	I_{CC2}	15	mA	1, 2
STANDBY CURRENT: TTL INPUT LEVELS V_{CC} power supply standby current (CE# = RP# = V_{IH}; Other inputs = V_{IL} or V_{IH})	I_{CC3}	2	mA	
STANDBY CURRENT: CMOS INPUT LEVELS V_{CC} power supply standby current (CE# = RP# = V_{CC} - 0.2V)	I_{CC4}	100	µA	
IDLE CURRENT (CE# ≤ 0.2V; f = 0Hz; Other inputs ≤ 0.2V or ≥ V_{CC} - 0.2V; RP# = V_{CC} - 0.2V; Array read mode)	I_{CC5}	2	mA	
DEEP POWER-DOWN CURRENT: V_{CC} SUPPLY (RP# = V_{SS} ±0.2V)	I_{CC6}	8	µA	
STANDBY OR READ CURRENT: V_{PP} SUPPLY (V_{PP} ≤ 5.5V)	I_{PP1}	±15	µA	
DEEP POWER-DOWN CURRENT: V_{PP} SUPPLY (RP# = V_{SS} ±0.2V)	I_{PP2}	5	µA	

NOTE: 1. I_{CC} is dependent on cycle rates.
2. I_{CC} is dependent on output loading. Specified values are obtained with the outputs open.

To determine the power consumption for the typical read operation, we can perform an analysis similar to the one performed to determine the I/O current for the microprocessor. Using the following equation:

$$I_{READ} = V \times C \times f \times \frac{(a+d)}{n}$$

where a + d = number of pins switching during a read operation and n = number of clocks per bus cycle. Using the input capacitance of the microprocessor for C, the resulting equation for current consumed as a result of the pin switching during the read operation, I_{READ}, is:

$$I_{READ} = (3.0V)(7\,pF)(13Mhz) \times \frac{16}{4} = 0.37mA$$

If we add up the leakage currents associated with the address inputs and the various control lines with the read current we just calculated, we get the following Table 12. MT28F400B3 Current Consumption.

Table 12. MT28F400B3 Current Consumption.

Pin	Condition	Current (mA)
A17:0	Input; Random (High=-100uA; Low=2mA)	18.9
CE	Input - Low	0.001
OE	Input - High	0.001
WP	Input - Low	0.001
BYTE	Input - Low	0.001
RP	Input - Low	0.001
WE	Input - Low	0.001
DQ:15:0	Random (see table)	15
Iread	Random (see calculation)	0.37
Total		**33.906**

4. Implementation

The 80L186EC microprocessor uses a multiplexed address and data bus architecture. Therefore, a latch is required to latch the address lines for the flash chip. This latch is described

in detail in the implementation section of the SRAM beginning on page 62. The same address lines that feed the SRAM are also wired to the address inputs of the flash memory. The circuit schematic for the memory circuit is provided in APPENDIX B – CIRCUIT SCHEMATICS. The microprocessor address lines A18:A1 are connected to the address pins A17:A0 of the flash chip. The microprocessor address line A19 is not connected to the FLASH chip. Instead, the $\overline{UCS}$ (upper chip select; active low) is wired to the $\overline{CS}$ (chip select; active low) of the MT28F400B3. The microprocessor must be programmed by the BIOS to drive the $\overline{UCS}$ pin low during any access to the memory range 80000h through FFFFFh.

The $\overline{RP}$ (reset/power down; active low) pin, the $\overline{WE}$ (write enable; active low), and the $\overline{BYTE}$ (enable single byte mode; active low) are all tied high through a pull-up resistor. This has the effect of (1) enabling the chip, (2) disabling all write accesses to the flash, and (3) forcing the chip into its 16-bit wide data mode. The $\overline{WP}$ (write protect; active low) is grounded. Tying this pin low prevents all write and erase operations from taking place in the boot block. Finally, the $\overline{OE}$ (output Enable; active low) is tied to the microprocessor $\overline{RD}$ (read; active low) line.

5. Timing

The timing diagram in Appendix C provides a detailed timing analysis of the address, data, and control lines between the 80L186EC CPU, the KM616U4000C SRAM, and the MT28F400B3 FLASH. The time critical parameters for the SRAM and the FLASH are (1) microprocessor address out to MC74LCS373 address latch out, (2) address latch setup and hold, (3) RAM data out to microprocessor data read, (4) microprocessor data out to SRAM write, and (5) RAM data out to high impedance. It is clear from the timing diagram in Appendix C that each of these critical time parameters can easily be met. The SRAM is discussed in detail in the following section entitled "SRAM" beginning on page 61.

The microprocessor is guaranteed to hold the address valid for 28.5nS on either side of the falling edge of ALE. The MC74LCX373 latch will propagate the address signal from the microprocessor on its data inputs through to its data outputs in 8.5nS. The latch requires a setup

and hold of 2.5nS before and 1.5nS after the falling edge of the ALE respectively. The address latches will hold the address for the FLASH and SRAM until the next rising edge on ALE occurs during the next bus cycle. The microprocessor will then drive the data lines, AD15:0, with data if required. This data will remain on the data bus until the next rising edge on ALE.

The next critical parameter is the SRAM/FLASH data out to microprocessor data read. The RAM device must be able to hold a valid output during the time the microprocessor expects to read data from the device. In this design, the microprocessor will expect to read the data from the multiplexed address/data bus during the end of the T3 bus sub-cycle. The RAM device must hold the data valid for at least 20nS of setup time and at least 3nS of hold time around the rising edge of the $\overline{RD}$ line. As evidenced by the timing diagram, the FLASH and the SRAM are both capable of meeting this requirement. Indeed, they will hold their respective outputs valid for about 110nS prior to and about 25nS after the rising edge of $\overline{RD}$. Similarly, the microprocessor must hold the data signal valid for the entire duration required for the SRAM to perform its write operation. The SRAM requires that the data be held valid for at least 30nS before the rising edge of the $\overline{WR}$ line. The microprocessor holds the data valid for approximately 153nS prior to this event.

The last critical timing parameter for the RAM devices is their ability to tri-state their outputs before the microprocessor attempts to drive the multiplexed address/data bus with a new address. Both the SRAM and the FLASH will return their outputs to the high-impedance state within 25nS of the rising edge of $\overline{RD}$. Since the next rising edge of ALE will not occur until 28.5nS after the rising edge of $\overline{RD}$ this parameter is also met.

The access speeds of the RAM devices are also of interest. Note that the FLASH device has an access time of 90nS while the SRAM has an access time of 70nS. The 90nS device is still fast enough for the system to functions properly. Indeed, the device could be much slower. The 70nS SRAM could likewise be slower and still meet the timing requirements. Samsung does manufacture slower SRAM chips and one of these slower chips should be used in the production of these devices to lower the total cost of the computer.

C. SRAM

The SRAM is responsible for providing all of the scratch pad and variable storage space for the BIOS, OS, and application program.

1. The Samsung KM616U4000

The 80L186EC microprocessor can make use of a 16-bit wide data bus. Therefore, the SRAM selected should also be capable of providing a 16-bit wide data path. This greatly limits our selection of chips. The SRAM used in this implementation is the Samsung KM616U4000CLI-L. This is a 256k x 16-bit Low Power Low Voltage CMOS SRAM. It is TTL compatible and uses tri-state outputs. It has a rated operating temperature range of –40 to 85°C.

2. Power

This chip is designed to function with an operating voltage between 2.7 and 3.3 volts and draws an average of 45mA. See Table 13. KM616U4000 Recommended Operating Conditions [Ref 15] and Table 14. KM616U4000 DC Operating Characteristics & Capacitance [Ref 15].

Table 13. KM616U4000 Recommended Operating Conditions [Ref 15].

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	Vcc	KM616V4000C Family KM616U4000C Family	3.0 2.7	3.3 3.0	3.6 3.3	V
Ground	Vss	All Family	0	0	0	V
Input high voltage	VIH	KM616V4000C, KM616U4000C Family	2.2	-	Vcc+0.3[2]	V
Input low voltage	VIL	KM616V4000C, KM616U4000C Family	-0.3[3]	-	0.6	V

Table 14. KM616U4000 DC Operating Characteristics & Capacitance [Ref 15].

Item	Symbol	Test Conditions	Min	Typ	Max	Unit
Input leakage current	ILI	VIL=Vss to Vcc	-1	-	1	mA
Output leakage current	ILO	CS=VIH or OE=VIH or WE=VIL VIO=Vss to Vcc	-1	-	1	mA
Operating power supply current	ICC	IIO=0mA, CS=VIL, VIN=VIL or VIH, Read	-	-	4	mA
Average operating current	ICC1	Cycle time=1ms, 100% duty, IIO=0mA CS£0.2V,VIN£0.2V or VIN³Vcc-0.2V	-	-	6	mA
	ICC2	Cycle time=Min, 100% duty, IIO=0mA, CS=VIL, VIN=VIH or VIL	-	-	45	mA
Output low voltage	VOL	IOL=2.1mA	-	-	0.4	V
Output high voltage	VOH	IOH=-1.0mA	2.2	-	-	V
Standby Current(TTL)	ISB	CS=VIH, Other inputs = VIL or VIH	-	-	0.3	mA
Standby Current(CMOS)	ISB1	CS³Vcc-0.2V, Other inputs=0~Vcc	-	-	15	mA
Capacitance						
Input Capacitance	CIN	VIN = 0V	-	-	8	pF
Input/Output Capacitance	CIO	VIO = 0V	-	-	10	pF

3. Implementation

Using the SRAM chips is complicated by the fact they require the address signal to be stable during the time the data output is being generated. The SRAM will maintain valid data for 15nS after the address changes. The microprocessor, however, uses multiplexed address and data lines with a four-clock bus cycle. Therefore, it applies the address during the first bus cycle, T1, and does not look for the data until the fourth cycle, T4. With a 13Mhz processor, each clock period is approximately 77.5nS long. Therefore, we need to latch the SRAM address line inputs. Latching the address line inputs requires additional chips and thus additional power consumption, specifically 3.15mA for the three MC74LCX373 octal transparent latches by Motorola.

The MC74LCX373 is a high performance low-voltage CMOS non-inverting octal transparent latch with 5 volt tolerant inputs and tri-state outputs. The LCX chip is designed to work with 2.7 to 3.6 volt operating supply voltage. The power consumption of this device consists primarily of two components, (1) the quiescent current consumption and (2) the internal parasitic capacitance current. The specification sheet for this device defines its maximum quiescent current, I_{PD}, to be 40μA and its typical power dissipation capacitance, C_{PD}, to be 25pF. Therefore the typical operating current, I_{CC}, can be calculated as $I_{CC} = I_{PD} + I_{CCS}$, where:

$$I_{PD} = 40\mu A$$

$$C_{PD} = \frac{I_{CCS}}{V_{CC} \bullet f} \Rightarrow I_{CC} = C_{PD}(V_{CC})(f)$$

$$\therefore I_{CCS} = (25pF)(3.0V)(13Mhz) = 0.975mA$$

Therefore,

$$I_{CC} = 40\mu A + 975\mu A = 1.05mA \quad \text{per latch.}$$

The latch address line outputs, A[18:1], are wired to each of the address inputs on the KM616U4000C. The address line A0 is not used because this chip provides a 16-bit wide data

output which fully populates the microprocessors data input, D15:D0. The address line A19 is wired to the SRAM chip select (active low), $\overline{CS}$. This activates the SRAM chip for all low address, 7FFFFh through 00000h, memory accesses and disables it for all high memory accesses, 80000h through FFFFFh. The microprocessors read, $\overline{RD}$, output is wired to this chips output enable, $\overline{OE}$, pin to allow the chip to transmit data during the data valid clock, T4, of the memory read bus cycle. The chips write enable, $\overline{WE}$, pin is wired to the microprocessors $\overline{WE}$ output. Finally, the SRAM chip has two other control inputs called Upper Byte, $\overline{UB}$, and Lower Byte, $\overline{LB}$. These inputs control which halves of the 16-bit wide data output are active at any given time. Both of these inputs are wired to ground through a pull down resistor to force the device into its 16-bit mode.

4. Timing

The AC operating characteristics of the KM616U4000 are provided in the following table. A detailed timing analysis has been completed to verify the ability of the CPU, memory, and latch circuits to perform properly.

Table 15. KM616U4000 AC Operating Characteristics [Ref 15].

Parameter List		Symbol	Speed Bins						Units
			70ns		85ns		100ns		
			Min	Max	Min	Max	Min	Max	
Read	Read cycle time	tRC	70	-	85	-	100	-	ns
	Address access time	tAA	-	70	-	85	-	100	ns
	Chip select to output	tCO	-	70	-	85	-	100	ns
	Output enable to valid output	tOE	-	35	-	40	-	50	ns
	$\overline{LB}$, $\overline{UB}$ valid to data output	tBA	-	35	-	40	-	50	ns
	Chip select to low-Z output	tLZ	10	-	10	-	10	-	ns
	Output enable to low-Z output	tOLZ	5	-	5	-	5	-	ns
	$\overline{LB}$, $\overline{UB}$ enable to low-Z output	tBLZ	5	-	5	-	5	-	ns
	Output hold from address change	tOH	10	-	10	-	15	-	ns
	Chip disable to high-Z output	tHZ	0	25	0	25	0	30	ns
	$\overline{OE}$ disable to high-Z output	tOHZ	0	25	0	25	0	30	ns
	$\overline{LB}$, $\overline{UB}$ disable to high-Z output	tBHZ	0	25	0	25	0	30	ns
Write	Write cycle time	tWC	70	-	85	-	100	-	ns
	Chip select to end of write	tCW	60	-	70	-	80	-	ns
	Address set-up time	tAS	0	-	0	-	0	-	ns
	Address valid to end of write	tAW	60	-	70	-	80	-	ns
	Write pulse width	tWP	55	-	60	-	70	-	ns
	Write recovery time	tWR	0	-	0	-	0	-	ns
	Write to output high-Z	tWHZ	0	25	0	25	0	30	ns
	Data to write time overlap	tDW	30	-	35	-	40	-	ns
	Data hold from write time	tDH	0	-	0	-	0	-	ns
	End write to output low-Z	tOW	5	-	5	-	5	-	ns
	$\overline{LB}$, $\overline{UB}$ valid to end of write	tBW	60	-	70	-	80	-	ns

See Appendix C for a detailed timing diagram of the address, data, and control lines between the 80L186EC CPU, the KM616U4000C SRAM, and the MT28F400B3 FLASH. See the discussion in the section entitled “Timing” under the section entitled “FLASH RAM” on page 53 for a detailed discussion of the critical timing parameters for the FLASH and SRAM.

VII. BIOS AND OS

The BIOS, or Basic Input Output System, is responsible for handling the initialization of the CPU and its supporting hardware. The "typical" BIOS consists of seven components. These components are (1) a Boot Vector, (2) a Power On Self Test (POST), (3) a BIOS compatibility table, (4) a set of BIOS Interrupt Service Routines, (5) a set of BIOS Device Service Routines, (6) a Boot Strap, and (7) some configuration tables. Several third party manufacturers build BOIS for Intel brand chips. The BIOS is hardware dependent and generally requires some modifications [Ref 16].

Because the scope of this thesis does not include the development of the software, it will not delve into the selection of the BIOS. However, several BIOS exist for the selected CPU and may be purchased from a variety of vendors. The vast majority of BIOS may be implemented in as little as 64Kbytes of ROM.

Table 16. BIOS Comparison [Ref 16].

Features	Phoenix Technologies	Award Software	System Soft	AMI	General Software	Eurosoft	Annabooks	USA Teknik
PCMCIA	Yes	Yes	Yes	Yes	Planned	Planned	Planned	Yes
FFS/FTL	Yes	Yes	Yes	Yes	Q1 95	Yes	No	Yes
APM	Yes	Yes	Yes	Yes	No	Yes	No	Yes
Min Size	12KB ROM	64KB ROM	N/A	64KBROM 1MB RAM	8KB ROM 4KB RAM	N/A	48KB ROM 4KB RAM	N/A
Free Source	Optional	Optional	No	Optional	Yes	Optional	Yes	Partial
Remote Floppy	No	No	No	No	Yes	Yes	Yes	Yes
Video/KBD to Serial	No	No	Yes	Yes	Yes	Yes	Yes	Yes
OEM Configurable	Yes	Yes	No	No	Yes	Yes	Yes	Yes
Debugger	Yes	Yes	No	Paradigm	Yes + SSI	Yes	Yes	No

The job of the BIOS is to initialize the hardware immediately after reset. Some of the jobs that will need to be done by the BIOS for this implementation are listed below:

1. Initialize address values for the $\overline{UCS}$ and the $\overline{LCS}$ pins. These chip select pins will select the appropriate memory chip during memory accesses. After reset, the $\overline{UCS}$ pin is initialized to go active during memory accesses in the range of FFC00h to FFFFFh.

2. Initialize the watchdog timer.
3. Reset I/O Ports.

VIII. THE GPS & EXTERNAL COMPUTER INTERFACES

Typically, the communications interface between two electronic devices is specified by defining four different aspects of the interface. These aspects are the (1) mechanical, (2) electrical, (3) functional, and (4) procedural characteristics of the interface. The interfaces between the PNCC and the two primary communicating devices are defined in the following section. The communications between the PNCC and GPS and the communications between the PNCC and the diagnostic computer will be serial and follow the V.24/EIA-232 standard.

The V.24/EIA-232 standard is built around the transmission of serial data over a single electrical conductor with additional conductors for handling control and ground signals. The V.24/EIA-232 standard supports full and half duplex transmissions. For more information on this and other serial data communications techniques, standards, and specifications see *Data and Computer Communications* by William Stallings [Ref 17]. The V.24/EIA-232 is one of the most widely used specifications and is thus the chosen specification for defining the communications interface for this device. The EIA-232 specification only defines the functional and procedural characteristics of the interface while V.24 references other standards for the electrical and mechanical characteristics. The V.24/EIA-232 specification defines the interface in the following standards documents:

1. Mechanical: ISO 2110
2. Electrical: V.28
3. Functional: V.24
4. Procedural: V.24

A. MECHANICAL SPECIFICATION

The mechanical characteristics of the specification pertain to the physical connection between the two devices. Typically, this will include a detailed definition of the physical plug, both male and female, as well as the cable that should be used to connect the devices together. The mechanical specification for the PNCS has the greatest flexibility of all the specifications. We will use the EIA-232-E specification for the purposes of this thesis. However, as will become apparent in the following sections, the PNCS will not use all of the signal lines defined by the EIA-

232-E standard. Indeed, the entire interface can easily be supported using only four signal lines (TX, RX, CTS, and GND) and thus could easily be made with a much smaller connector than the one described here. Figure 28 shows the pin assignments for the mechanical interface as defined by the V.24 specification. This connector is commonly called a DB25-D type connector. The exact dimensions for this connector are defined in ISO 2110.

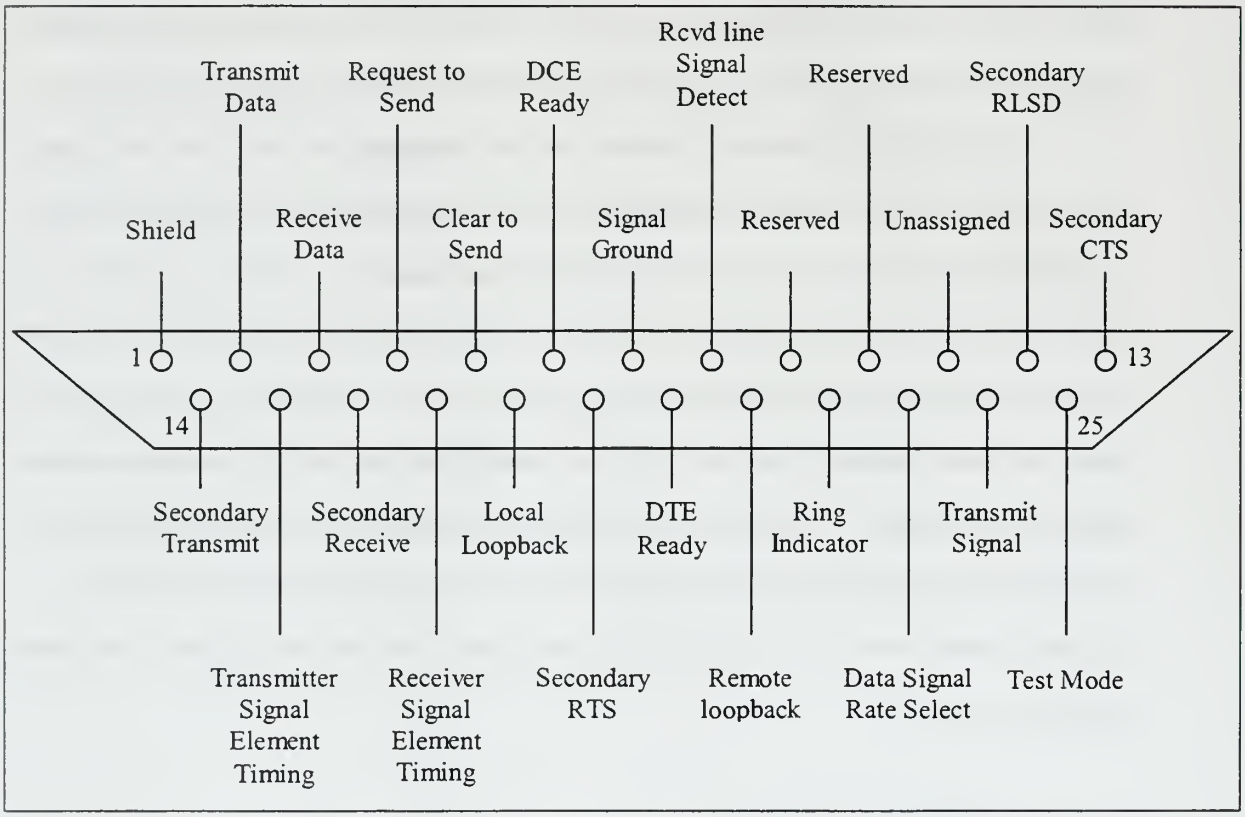

Figure 28. EIA-232-E Mechanical Connector Pin Assignments.

B. PROCEDURAL & FUNCTIONAL SPECIFICATIONS

The procedural and functional specifications of the interface are well defined in the EIA-232 standard. Therefore replication here is unnecessary. Table 17 lists the names of the circuits and their respective V.24 and EIA-232 designators. This table is included here for reference. For more detailed information about the V.24 or EIA-232 functional and/or procedural specifications see the appropriate commercially available standards document or reference 17.

Table 17. V.24/EIA-232 Circuits.

V.24	EIA-232	Name
103	BA	Transmitted data
104	BB	Received data
118	SBA	Secondary transmitted data
104	SBB	Secondary received data
105	CA	Request To Send (RTS)
106	CB	Clear To Send (CTS)
107	CC	DCE Ready
108.2	CD	DTE Ready
125	CE	Ring Indicator
109	CF	Received Line Signal Detector
110	CG	Signal Quality Detector
111	CH	Data Signal Rate Selector
112	CI	Data Signal Rate Selector
133	CJ	Ready for Receiving
120	SCA	Secondary Request to Send
121	SCB	Secondary Clear to Send
122	SCF	Secondary Received Line Signal Detector
140	RL	Remote Loopback
141	LL	Local Loopback
142	TM	Test Mode
113	DA	Transmitter signal element timing
114	DB	Transmitter signal element timing
115	DD	Receiver signal element timing
102	AB	Signal Ground

C. ELECTRICAL SPECIFICATION

The electrical specification defines the signaling between the two devices. Figure 20 shows a typical electrical signaling waveform for serial communications. The V.24 specification defines a voltage level of less than –3 volts to be a binary 1 and a voltage greater than +3 volts to be a binary 0. The specification defines the interface to be effective for signaling rates up to 20k bits/second for connector lengths less than 15 meters.

For the purposes of this thesis it is important to explore the relationship between the standards specification and the capabilities of the Intel 80L186EC microprocessor to adhere to the standard.

D. SERIAL INTERFACE IMPLEMENTATION

The 80L186EC supports two independent serial I/O ports. However, these ports are CMOS outputs and should not be connected directly to any external devices. A line buffer or transceiver is required to protect the microprocessor and to perform voltage level conversions to allow interfaces with a variety of peripheral equipment. The MAX3223CAP RS-232 Transceiver by Maxim Integrated Products provides this capability for the PNCS CPU. See reference 18 for more information regarding the MAX322x family of transceivers.

The MAX3223 is a 3.0V EIA-232 and V.28/V.24 transceiver with two transmit lines and two receive lines. The device will generate true EIA-232 standard voltage levels from a 3.0V to 5.5V supply. This design will employ two of the devices, one for each serial port, to allow for the support of the clear-to-send pins. These devices have an AutoShutdown™ feature which will cause the device to enter a very low-power mode when it is not in use. These transceivers will sense their inputs for 30nS. If no activity is detected during that time, they will enter an auto shutdown mode in which they draw only 1μA. Table 18 and Table 19 are taken from the technical data sheets for this part and provide the DC Operating Characteristics for the transceivers. This is particularly convenient in the case of the diagnostic computer port. This port will only be used very infrequently. As a result, the AutoShutdown™ feature will cause the transceiver connected to that port to draw only 1μA for the majority of its time. Only when a diagnostic computer is actually connected to the PNCS will that transceiver begin to draw maximum current. See Table 18 and Table 19 to determine the worst case current the devices will draw.

Table 18. MAX3223 DC Operating Characteristics [Ref 18].

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS (V_{CC} = 3.3V or 5.0V, T_A = +25°C)							
Supply Current, AutoShutdown		FORCEON = GND, $\overline{FORCEOFF}$ = Vcc, all R_IN open			1.0	10	µA
Supply Current, Shutdown		$\overline{FORCEOFF}$ = GND			1.0	10	µA
Supply Current, AutoShutdown Disabled		FORCEON = $\overline{FORCEOFF}$ = Vcc, no load			0.3	1	mA
LOGIC INPUTS							
Input Logic Threshold Low		T_IN, $\overline{EN}$, FORCEON, $\overline{FORCEOFF}$				0.8	V
Input Logic Threshold High		T_IN, $\overline{EN}$, FORCEON, $\overline{FORCEOFF}$	Vcc = 3.3V	2.0			V
			Vcc = 5.0V	2.4			
Transmitter Input Hysteresis					0.5		V
Input Leakage Current		T_IN, $\overline{EN}$, FORCEON, $\overline{FORCEOFF}$			±0.01	±1	µA
RECEIVER OUTPUTS							
Output Leakage Current		R_OUT, receivers disabled			±0.05	±10	µA
Output Voltage Low		I_{OUT} = 1.6mA				0.4	V
Output Voltage High		I_{OUT} = -1.0mA		Vcc - 0.6	Vcc - 0.1		V
AUTOSHUTDOWN (FORCEON = GND, $\overline{FORCEOFF}$ = Vcc)							
Receiver Input Threshold to $\overline{INVALID}$ Output High		Figure 5a	Positive threshold			2.7	V
			Negative threshold	-2.7			
Receiver Input Threshold to $\overline{INVALID}$ Output Low		Figure 5a		-0.3		0.3	V
$\overline{INVALID}$ Output Voltage Low		I_{OUT} = 1.6mA				0.4	V
$\overline{INVALID}$ Output Voltage High		I_{OUT} = -1.0mA		Vcc - 0.6			V

Table 19. MAX3223 DC Operating Characteristics (cont) [Ref 18].

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Receiver Positive or Negative Threshold to $\overline{INVALID}$ High	t_{INVH}	V_{CC} = 5V, Figure 5b			1		µs
Receiver Positive or Negative Threshold to $\overline{INVALID}$ Low	t_{INVL}	V_{CC} = 5V, Figure 5b			30		µs
Receiver or Transmitter Edge to Transmitters Enabled	t_{WU}	V_{CC} = 5V, Figure 5b			100		µs
RECEIVER INPUTS							
Input Voltage Range				-25		25	V
Input Threshold Low		T_A = +25°C	V_{CC} = 3.3V	0.6	1.2		V
			V_{CC} = 5.0V	0.8	1.5		
Input Threshold High		T_A = +25°C	V_{CC} = 3.3V		1.5	2.4	V
			V_{CC} = 5.0V		1.8	2.4	
Input Hysteresis					0.5		V
Input Resistance				3	5	7	kΩ
TRANSMITTER OUTPUTS							
Output Voltage Swing		All transmitter outputs loaded with 3kΩ to ground		±5	±5.4		V
Output Resistance		V_{CC} = V_+ = V_- = 0, T_{OUT} = ±2V		300	10M		Ω
Output Short-Circuit Current						±60	mA
Output Leakage Current		V_{OUT} = ±12V, V_{CC} = 0 or 3V to 5.5V, transmitters disabled				±25	µA
MOUSE DRIVEABILITY (MAX3243E)							
Transmitter Output Voltage		T1IN = T2IN = GND, T3IN = V_{CC}, T3OUT loaded with 3kΩ to GND, T1OUT and T2OUT loaded with 2.5mA each		±5.0			V
ESD PROTECTION							
R_IN, T_OUT		IEC 1000-4-2 Air-Gap Discharge			±15		kV
		IEC 1000-4-2 Contact Discharge			±8		
		Human Body Model			±15		

Based on the data from these tables, the current consumption of these devices can be determined. Assume that the total current consumption consists primarily of the devices quiescent current I_{CCQ} and the current consumed by the device receiver outputs in both their high and low states equally, I_{HIGH} and I_{LOW}. Then the total current becomes

$$I_{CC} = I_{CCQ} + 2\left(\frac{I_{HIGH} + I_{LOW}}{2}\right) = 1.0mA + 2\left(\frac{1.6mA + 1.0mA}{2}\right) = 3.6mA$$

IX. TACTOR ARRAY INTERFACE

A. THE TACTOR

The tactor is a vibration device designed to provide a tactile stimulus to the human body. The tactors we will consider were developed for the Naval Aerospace Medical Research Laboratory (NAMRL) in support of their Tactile Situational Awareness System (TSAS), see the Tactile Situational Awareness System web page [Ref 19] for more information about TSAS and the NAMRL. The design of a Tactor is beyond the scope of this thesis. However, for more information regarding the tactor and some control electronics currently under development, see reference 20 and reference 21 or the technical data sheets for the tactors provided in APPENDIX F – TECHNICAL DATA SHEETS.

B. TACTOR INTERFACE IMPLEMENTATION

The tactor array is worn by the user and consists of eight independently controlled tactors. Because the tactors are not located adjacent to the computer and power supply, the size of the connecting cable must be taken into account. Figure 29 below shows how up to nine tactors could be controlled using as few as six control lines. The tactors are controlled by either applying electrical ground to one of the ground control points, TC_A, TC_B, or TC_C, and subsequently applying power, TPWR, to the opposite power control point, TC_0, TC_1, or TC_2.

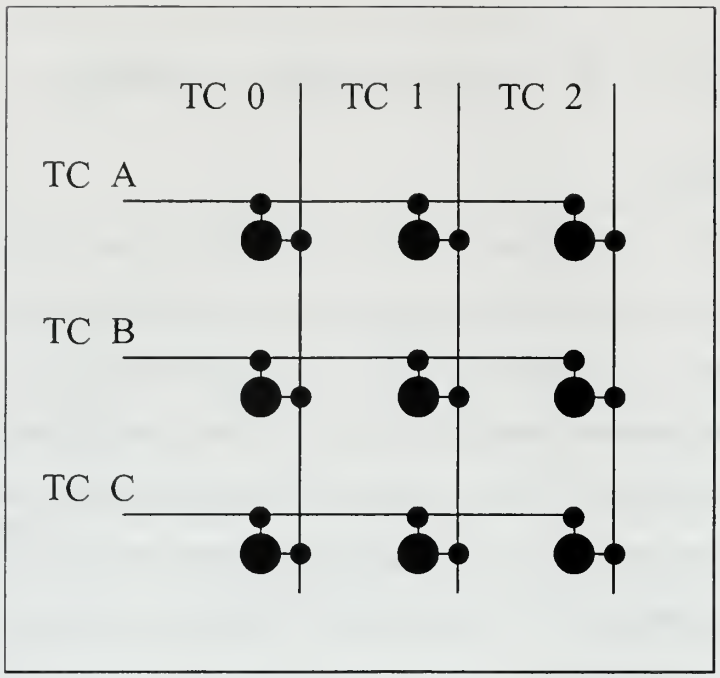

Figure 29. Nine Tactor Array using Six Control Lines.

The tactors, unlike the rest of this design, require a substantial current flow, 250mA rms, for them to operate. Clearly, the microprocessor cannot provide these kinds of levels. Therefore, the actual implementation will require some additional circuitry in the form of power transistors and transistor drivers. See the circuit schematic labeled "Tactor Control Circuit" in APPENDIX B – CIRCUIT SCHEMATICS.

1. Tactor Select Logic

The purpose of the tactor select logic is to provide a mechanism by which the number of electrical lines needed to control the eight tactors can be reduced. To accomplish this, the CPU software controls the tactor select logic by generating a six-bit digital word and presenting it on its programmable output pins. The hardware design is such that the CPU may control up to eight (potentially nine) tactors independently through the use of these six different control lines labeled, TC_0, TC_1, TC_2, TC_A, TC_B, and TC_C. The lines TC_A:C are used to control the rows of tactors by switching the electrical ground, GND, in and out, while the lines TC_0:2 are used to control the columns of tactors by switching power, TPWR, in and out. For example, to turn on

only tactor number B2, the computer would provide the following six-bit digital word: 010010. To activate all tactors in row 0, the word would look like this: 100111.

2. Tactor Driver Circuit

The tactor driver circuit must be capable of accepting low voltage CMOS inputs and driving the relatively high current demands of the tactors. Therefore, this circuit consists of two basic elements. It uses a CMOS low-voltage MOSFET driver in conjunction with an array of low-voltage N-Channel MOSFETs. N-Channel MOSFETs must be used because the P-Channel devices do not have guaranteed $R_{DS(ON)}$ with $V_{GS} \leq 3.3$ volts.

The Linear Technology device LTC1157 is a 3.3 Volt Dual Micro-power High-Side/Low-Side MOSFET Driver. This device uses internal capacitors in a charge pump configuration to generate a 4.7V MOSFET drive signal from a standard CMOS input when driven by a 3.0 volt V_{CC}. The LTC1157 has a very low quiescent current when on, 160uA max for V_{CC} = 3.3V, and is capable of driving the gate of the N-Channel MOSFET power transistors which in turn drive the tactors. Table 20 provides the DC Operating Characteristics for the LTC1157 device.

Table 20. LTC1157 DC Operating Characteristics [Ref 22].

SYMBOL	PARAMETER	CONDITIONS		LTC1157C MIN	TYP	MAX	UNITS
I_Q	Quiescent Current OFF	V_S = 3.3V, $V_{IN1} = V_{IN2}$ = 0V (Note 1)			3	10	µA
	Quiescent Current ON	V_S = 3.3V, V_{IN} = 3.3V (Note 2) V_S = 5V, V_{IN} = 5V (Note 2)			80 180	160 400	µA µA
V_{INH}	Input High Voltage		●	70% × V_S			V
V_{INL}	Input Low Voltage		●			15% × V_S	V
I_{IN}	Input Current	0V ≤ V_{IN} ≤ V_S	●			±1	µA
C_{IN}	Input Capacitance				5		pF
$V_{GATE} - V_S$	Gate Voltage Above Supply	V_S = 3V V_S = 3.3V V_S = 5V	● ● ●	4.0 4.5 7.5	4.7 5.4 8.8	6.5 7.0 12.0	V V V
t_{ON}	Turn-ON Time	V_S = 3.3V, C_{GATE} = 1000pF Time for $V_{GATE} > V_S + 1V$ Time for $V_{GATE} > V_S + 2V$		 30 75	 130 240	 300 750	 µs µs
		V_S = 5V, C_{GATE} = 1000pF Time for $V_{GATE} > V_S + 1V$ Time for $V_{GATE} > V_S + 2V$		 30 75	 85 230	 300 750	 µs µs
t_{OFF}	Turn-OFF Time	V_S = 3.3V, C_{GATE} = 1000pF Time for $V_{GATE} < 0.5V$		 10	 36	 60	 µs
		V_S = 5V, C_{GATE} = 1000pF Time for $V_{GATE} < 0.5V$		 10	 31	 60	 µs

Linear Technology Corporation recommends that the supply pin of the LTC1157 should never be driven below ground. To minimize the effect of this eventuality, a 300-ohm resistor is placed in series between the LTC1157 ground pin and ground. This will limit the current to less than 12mA for a 3.3V source in the event batteries are inserted incorrectly. Because the device draws very little current during normal operation the voltage drop across the reverse battery protection resistor is low. The worst case drop is $V = (160\mu A)(300\Omega) = 48mV$. See reference 22 for more details on the LTC1157.

The MTD3055VL N-Channel power MOSFET by Motorola is used in this circuit to act as the switch for engaging the power and ground for the tactors. Three MOSFETs are used to switch the power and three are used to switch the ground in and out. Table 21 provides the electrical characteristics of the MOSFET. Notice that the device draws almost no current through either the gate, I_{DDS} = 100μA, or the body, I_{GSS} = 100ηA. When on, the gate to source voltage is driven by the LTC1157 to approximately 4.7V, at which the MOSFET is capable of delivering about 15 or 16 Amps (see Figure 30. MTD3055VL I_D vs V_{GS}). Since the MOSFET is driven directly from the battery supply, via TPWR, V_{DS} will be between 4.0V and 4.5V. Which, according to Figure 31. MTD3055VL I_D vs V_{DS}, will allow the device to deliver nearly 22A. Clearly, the MTD3055VL can be driven by the LTC1157 and provide adequate current to drive the tactors. The voltage drop across the devices needs to be considered as well. According to Figure 32. MTD3055VL $R_{DS(on)}$ vs I_D, the $R_{DS(ON)}$ for this device, under these circumstances, is going to be about 0.11 ohms. The resulting voltage drop will then be about

$$V_{DS} = I_D \times R_{DS(on)} = (250mA)(0.11\Omega) = 27.5mV.$$

Table 21. MTD3055VL Electrical Characteristics [Ref 23].

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc)	$V_{(BR)DSS}$	60	—	—	Vdc
Temperature Coefficient (Positive)		—	62	—	mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
(V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		—	—	100	
Gate–Body Leakage Current (V_{GS} = ±15 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	100	nAdc
ON CHARACTERISTICS (1)					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 250 μAdc)	$V_{GS(th)}$	1.0	1.6	2.0	Vdc
Threshold Temperature Coefficient (Negative)		—	3.0	—	mV/°C
Static Drain–Source On–Resistance (V_{GS} = 5.0 Vdc, I_D = 6.0 Adc)	$R_{DS(on)}$	—	0.12	0.18	Ohm
Drain–Source On–Voltage (V_{GS} = 5.0 Vdc)	$V_{DS(on)}$				Vdc
(I_D = 12 Adc)		—	1.6	2.6	
(I_D = 6.0 Adc, T_J = 150°C)		—	—	2.5	
Forward Transconductance (V_{DS} = 8.0 Vdc, I_D = 6.0 Adc)	g_{FS}	5.0	8.8	—	mhos

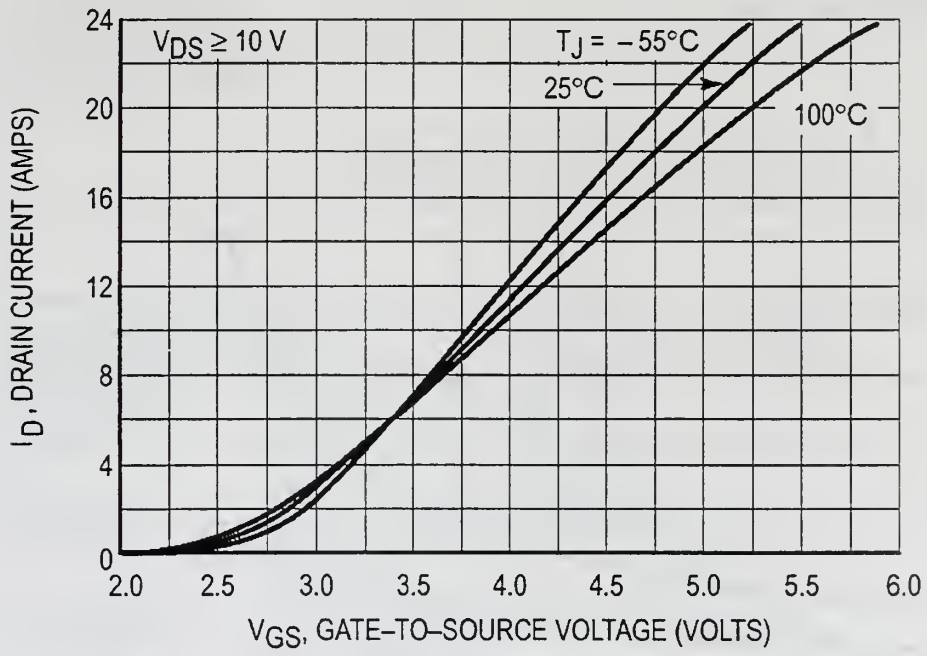

Figure 30. MTD3055VL I_D vs V_{GS}.

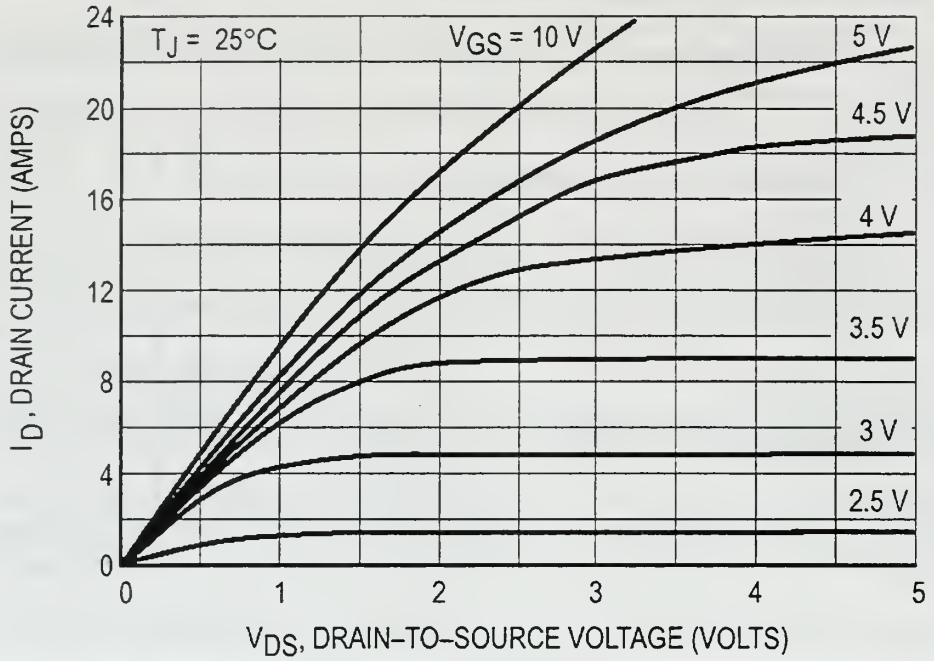

Figure 31. MTD3055VL I_D vs V_{DS}.

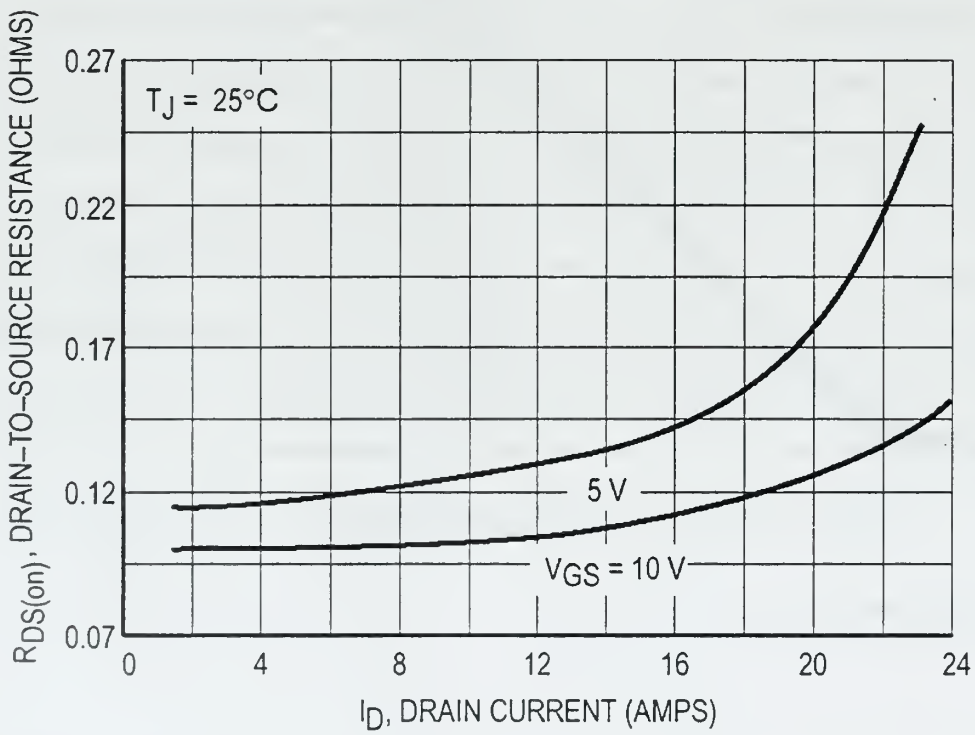

Figure 32. MTD3055VL $R_{DS(on)}$ vs I_D.

C. ALTERNATE SOLUTION: ENGINEERING ACOUSTICS, INC.

An alternate solution is to procure both the tactor and its associated drive circuitry from a vendor, like Engineering Acoustics, Inc. (EAI). EAI manufactures a device they call a Vibrotactile Transducer. Their model C1-97, see reference 20, is a small (1.26" diameter x 0.46" high), light weight (26 grams) device designed to provide a vibrotactile stimulus through direct contact with the human body. The electrical characteristics of this tactor (vibrotactile transducer) are given in Table 22. EAI C1-97 Vibrotactile Transducer Electrical Characteristics [Ref 20]. The electrical characteristics of an optional drive amplifier, also provided by EAI, are given in Table 23. EAI C1-97 Optional Drive Amplifier Electrical Characteristics [Ref 20]

Table 22. EAI C1-97 Vibrotactile Transducer Electrical Characteristics [Ref 20].

Vibrotactile Transducer	
Series Resistance	12 Ohms
Series Inductance	1.7 mH
Resonance Frequency	200 Hz
Recommended Stimulus	Sine wave tone bursts 50 to 200 ms duration in 100 to 250 Hz frequency range at current levels up to 250mA rms max.

Table 23. EAI C1-97 Optional Drive Amplifier Electrical Characteristics [Ref 20].

Drive Amplifier	
Input Power	6Vdc at 250mA
Input Signal	TTL activated on or off
Output	Bi-Polar switched signal; 250mA rms out into 12 ohm load with 40% duty cycle
Frequency	Manually selectable; 120 to 280 Hz
Driver Configuration	H-bridge switching amp with TTL activated output gates
Power Levels	Full power and -6dB nominal, TTL selectable
PWB Size	2.3" x 2.6" x 0.25"

The principle disadvantage with this approach is that a separate drive is required for each tactor and the drives will need to be mounted next to the tactors in order to take advantage of the reduced transmission wire set. This makes the vest larger and more cumbersome. Also, the drivers require a 6V input. Our system was designed to use a 4.5V battery source. However, because a separate power line, TPWR, which comes directly from the battery drives the tactors,

we can simply use four 1.5V batteries to provide the proper voltage at the tactors. Additionally, the MAX603 power regulator, which controls V_{CC}, is capable of accepting an input voltage of up to 11.5V. Therefore, no change in the power control circuit is required to support the higher tactor control voltage supplies by TPWR.

The most significant problem, of course, is the current consumption of the devices, 250mA rms. If we limit the number of simultaneously active tactors to 1 and limit the number of pulses sent to the tactor to 50 (i.e. a 200 ms tone burst) then the resulting current consumption becomes 125mA. If we further limit the frequency of stimulation by inserting a 1-second delay between subsequent tactor updates, we can reduce the current consumption to a more manageable time averaged current of $\frac{125mA}{2\text{sec}} = 62.5mA$.

X. CONCLUSIONS AND RECOMMENDATIONS

A. Conclusions

The expected battery lifetime of the system is highly dependent on the implementation of the software and the frequency of tactor usage. Because the tactors can draw nearly twice the current as the microprocessor and memory chips combined, their usage should be as limited as possible. However, if we hold to the assumptions of usage made in this thesis, we can come to some conclusions about how long the system is expected to last given various battery sources. For the purpose of this thesis, we are considering using AA type batteries. Figure 13, Figure 14, and Figure 15 provide data on how long a AA battery can be expected to last. Table 24. PNCC Device List, in APPENDIX A – DEVICE LIST of this thesis, provides us with the total current the PNCS will consume during normal operations, just over 200mA. Based on the curves in the figures this means that we can expect the system to last between 5 and 6 hours with either a NiMH or an alkaline battery pack. The data clearly shows that lithium batteries not only have a better discharge profile they will also hold a higher voltage for a longer time. Figure 15 shows that a lithium battery was able to power an 11.3 ohm load for about $1-\frac{17.5}{13}=35\%$ longer (17.5 hours vs 13 hours) than an alkaline battery. Our system has a lower equivalent resistance and draws much more current so the discharge curves will look slightly different. However, it is a reasonable approximation to infer that using lithium batteries in our design will extend the life of the system from 5 or 6 hours to something more like 8 hours.

One of the advantages of using the FLASH memory is the ability to reprogram the chip. Because the application program will be stored in the FLASH memory, it is theoretically possible to implement a feature in the design which will allow the FLASH to be reprogrammed "in-circuit." A future modification of this design would include that capability. This FLASH device can be reprogrammed with a 3.3V V_{PP}.

This system was designed to operate at 3.0V. Great care was taken to select real chips with the appropriate voltage and timing tolerances. However, in some cases (i.e. the MT28F400B3 FLASH Memory by Micron) the voltage margin is very narrow. The operating

voltage range for the FLASH memory is 3.0V to 3.6V. This provides almost no margin for error in the selection of the power supply devices. The MAX603 linear regulator will provide a 3.0V output. However, the specific output of the device is highly dependent on the exact values of the resistors used to "program" the devices output voltage. As a result, 1% tolerance resistors must be used if the entire system is likely to function properly. These kinds of margin tolerances should be avoided whenever possible.

The microprocessor used in this design employs a multiplexed address bus. This requires that additional hardware be added to latch the address for accesses to data in memory. A future design should use a microprocessor that does NOT employ a multiplexed address/data bus. This will eliminate the need for the additional hardware required to implement an address latch. This reduces the component count, and cost, by three chips and the current consumption by 1.05mA per latch or 3.15mA. A current savings of 3.15mA is significant considering the low-power nature of portable systems in general.

A 70nS SRAM chip was chosen for this design. However, from the timing diagram in Appendix C, it is clear that a slower (perhaps 90ns or 100ns) SRAM chip will still be adequate. Samsung manufactures an 85nS version as well as a 100nS version of the same chip. A slower chip will likely be less expensive and thus should be used over the faster 70nS chip for production.

Future chips will require lower operating voltage. Some memory chips are or will soon be available with operating ranges between 1.8v and 2.7v. Once these chips are reliably available the power supply should be redesigned to provide an additional voltage level for these types of chips. This would allow for the "creative re-design" of certain portion of this system to reduce the current consumption. However, the most expensive component, with respect to current, is the tactor. Significant attention should be paid to the development of tactors with lower current requirements.

Finally, although these tactors are presented in the literature as being small and lightweight, without question there exist tactors that are smaller, lighter, and consume less current. Consider the tactors used in commercial pagers. In all likelihood the tactors designed

for the NAMRL were designed to be reliable in very harsh environments. Additional research should be engaged to locate smaller, lighter, and lower power tactors. This is probably the first area of improvement that will greatly extend the expected battery life of this system.

B. Recommendations

Several things can be done to increase the battery life, (1) increase the number of batteries, (2) increase the size of the batteries (i.e. use C or D cells), (3) use a slower frequency microprocessor, (4) implement a design with more 1.8V and 2.7V chips, (5) reduce the usage of the tactors, or (6) implement lower power tactors. The most advantageous is probably number six. Additional research should be engaged to locate smaller, lighter, and lower power tactors.

A future design should use a microprocessor that does NOT employ a multiplexed address/data bus. This reduces the component count, and cost, by three chips and the current consumption by 1.05mA per latch or 3.15mA. A slower SRAM chip will suffice and should be used in place of the faster chip identified in this design.

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APPENDIX A – DEVICE LIST

Table 24. PNCC Device List.

Part Number	Device	Device No	Purpose	Manufacturer	Manufacturer ID	Operating Voltage		Icc (mA)
						Minimum (Volts)	Maximum (Volts)	
						3.0	3.3	206.893
1	Microprocessor	1	Microprocessor	Intel	80L186EC-13	2.7	5.5	54
2	256k x 16-bit SRAM	1	Scratch Pad	Samsung	KM616U4000C	2.7	3.3	45
3	256k x 16-bit FLASH	1	Non-Vol Storage	Micron	MT28F4000B3	3.0	3.6	33.9
4	Octal Latch	1	Address Latch	Motorola	MC74LCX373	2.7	3.6	1.05
5	Octal Latch	2	Address Latch	Motorola	MC74LCX373	2.7	3.6	1.05
6	Octal Latch	3	Address Latch	Motorola	MC74LCX373	2.7	3.6	1.05
7	Dual MOSFET Driver	1	Tactor Drive Signal	Linear Technology	LTC1157	2.7	5.5	0.16
8	Dual MOSFET Driver	2	Tactor Drive Signal	Linear Technology	LTC1157	2.7	5.5	0.16
9	Dual MOSFET Driver	3	Tactor Drive Signal	Linear Technology	LTC1157	2.7	5.5	0.16
10	N-Channel MOSFET	1	Tactor Drive Signal	Motorola	MTD3055VL	-15.0	15.0	0.100
11	N-Channel MOSFET	2	Tactor Drive Signal	Motorola	MTD3055VL	-15.0	15.0	0.100
12	N-Channel MOSFET	3	Tactor Drive Signal	Motorola	MTD3055VL	-15.0	15.0	0.100
13	N-Channel MOSFET	4	Tactor Drive Signal	Motorola	MTD3055VL	-15.0	15.0	0.100
14	N-Channel MOSFET	5	Tactor Drive Signal	Motorola	MTD3055VL	-15.0	15.0	0.100
15	N-Channel MOSFET	6	Tactor Drive Signal	Motorola	MTD3055VL	-15.0	15.0	0.100
16	Dual Switch Debouncer	1	On/Off Debounce	MAXIM	MAX6817	2.7	5.5	0.020
17	Voltage Regulator	1	Voltage Regulation	MAXIM	MAX603C	2.7	11.5	0.035
18	uP Supervisor	1	Reset Performance	MAXIM	MAX6319HL	1.0	5.5	0.008
19	RS-232 Tranceiver	1	Level Conversion	Maxim	MAX3223CAP	3.0	5.5	3.6
20	RS-232 Tranceiver	2	Level Conversion	Maxim	MAX3223CAP	3.0	5.5	3.6
21	Tactor	1	Tactile Stimulus	EAI	C1-97	3.0	6.0	62.5

Table 25. PNCC Device Costs.

Manufacturer Part Number	Manufacturer	Description	Supplier	Quantity	Price ($ea)	Total Cost ($)
80L186EC-13	Intel					
C1-97	EAI	Tactor	EAI	8		
KM616U4000C	Samsung					
LTC1157	LTI			3		
MAX3223CAP	Maxim		Maxim-ic	2	2.86	5.72
MAX5102	Maxim	Digital to Analog Coverter	Maxim-ic	1	12.04	12.04
MAX603CPA	Maxim	Linear Regulator	Maxim-ic	1	2.98	2.98
MAX6319HL	Maxim	Microprocessor Supervisor	Maxim-ic	1	5.98	5.98
MAX6817	Maxim	Switch Debouncer	Maxim-ic	1	5.98	5.98
MC74LCX373	Motorola	Octal Latch		3		
MPT60N06	Motorola	Power MOSFET	Newark	6	2.32	13.92
MT28F4000B3	Micron	FLASH RAM				
Total						46.62

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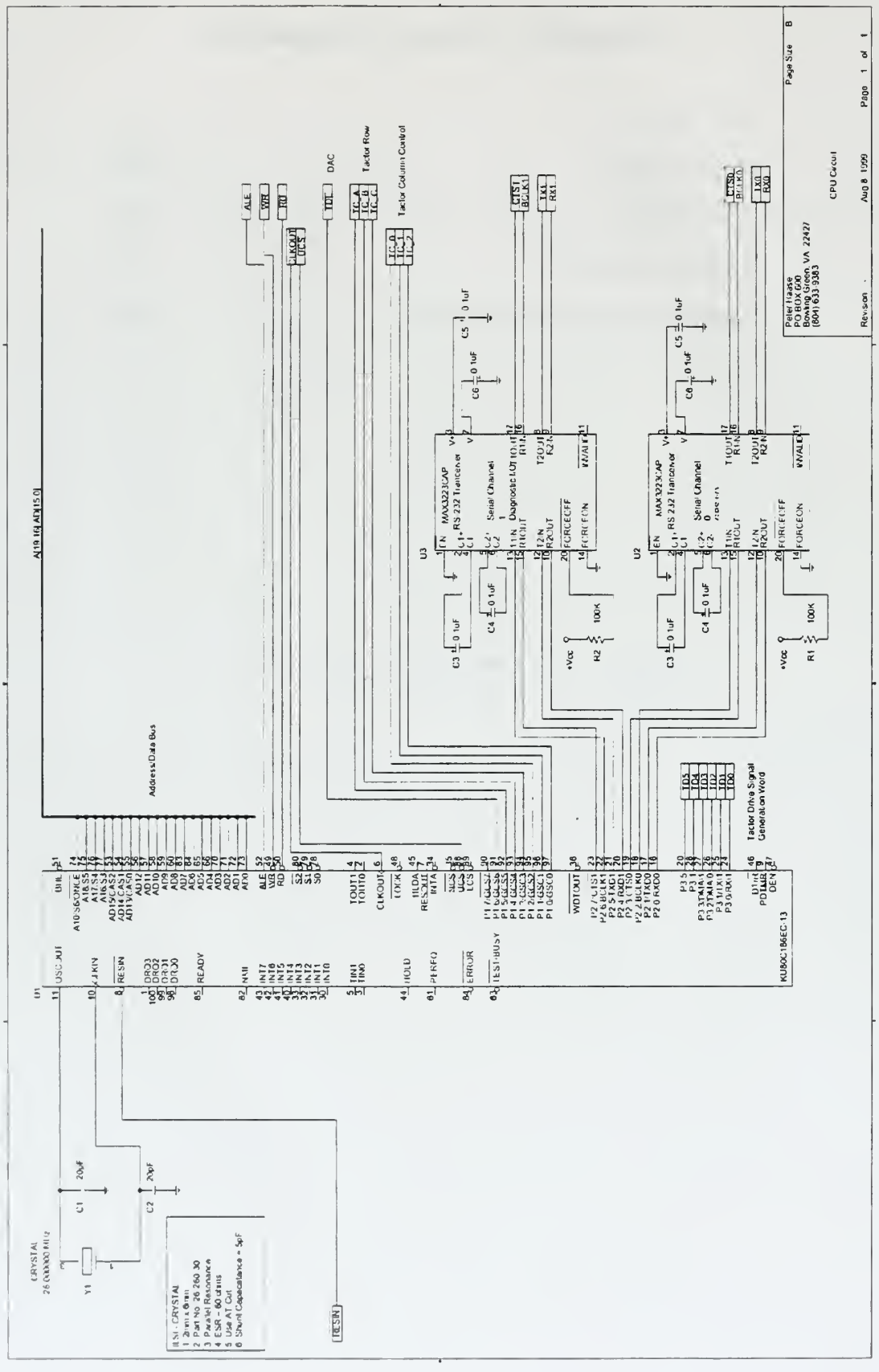
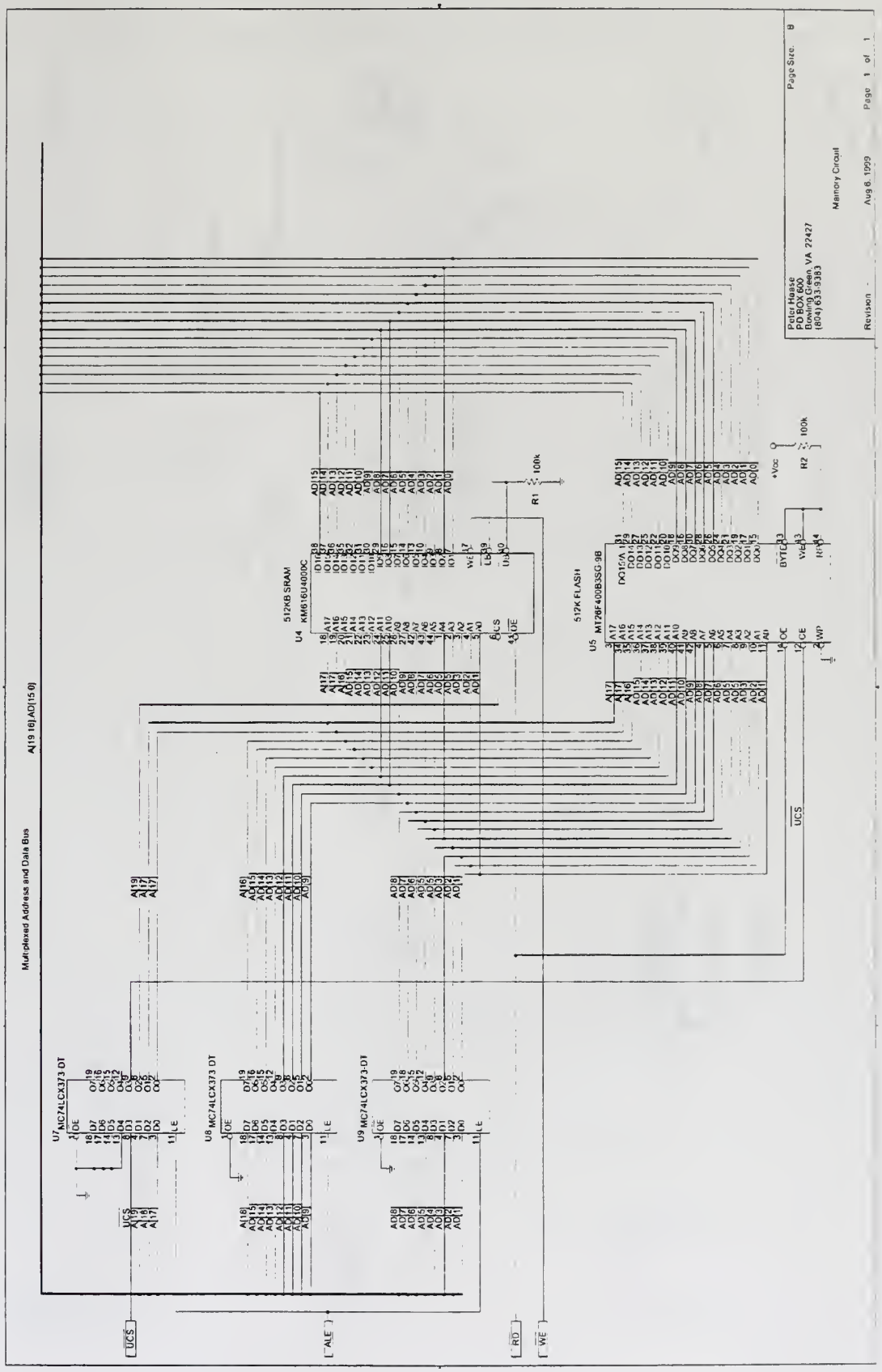
APPENDIX B – CIRCUIT SCHEMATICS

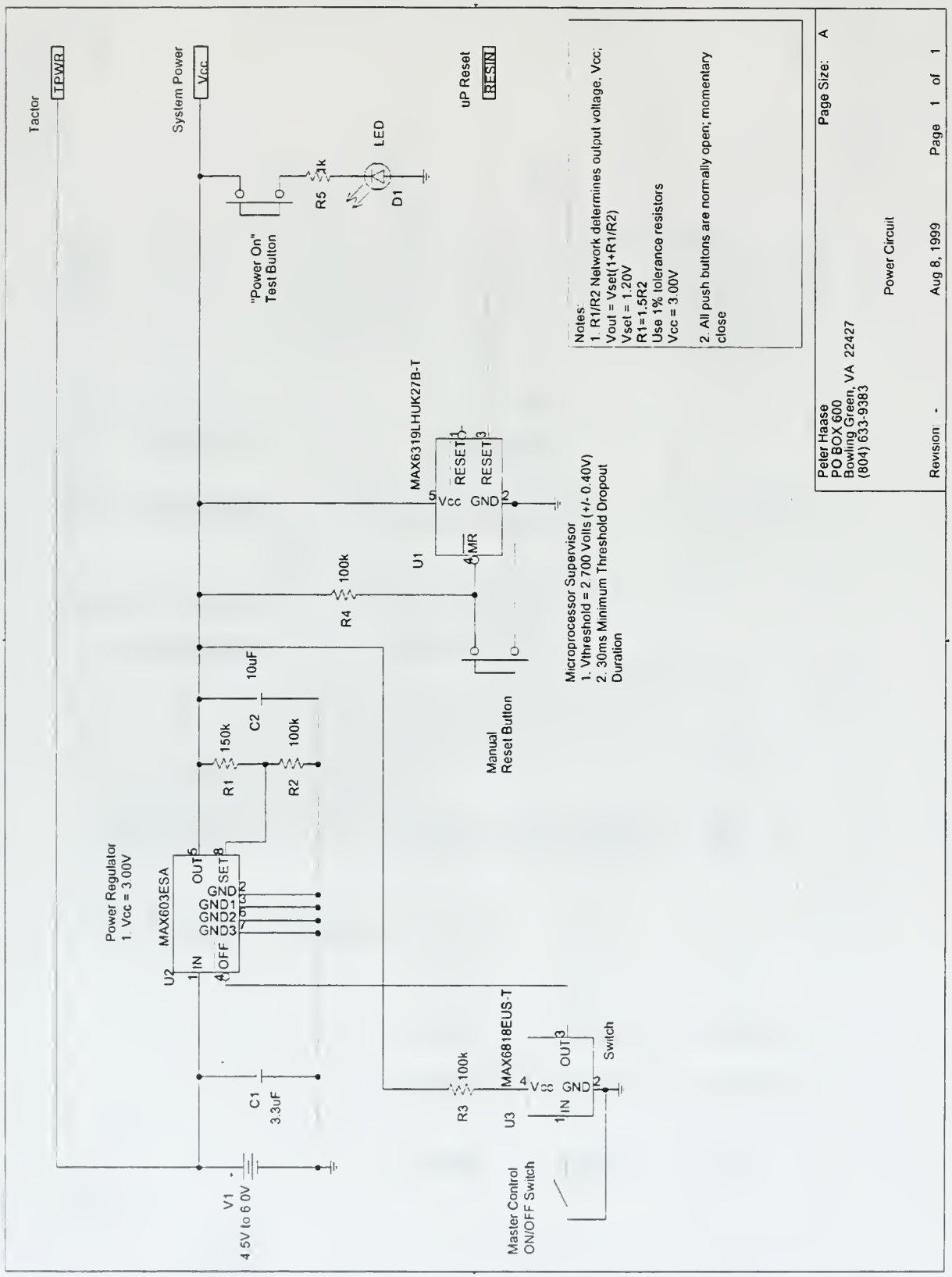
Appendix B – CPU Circuit



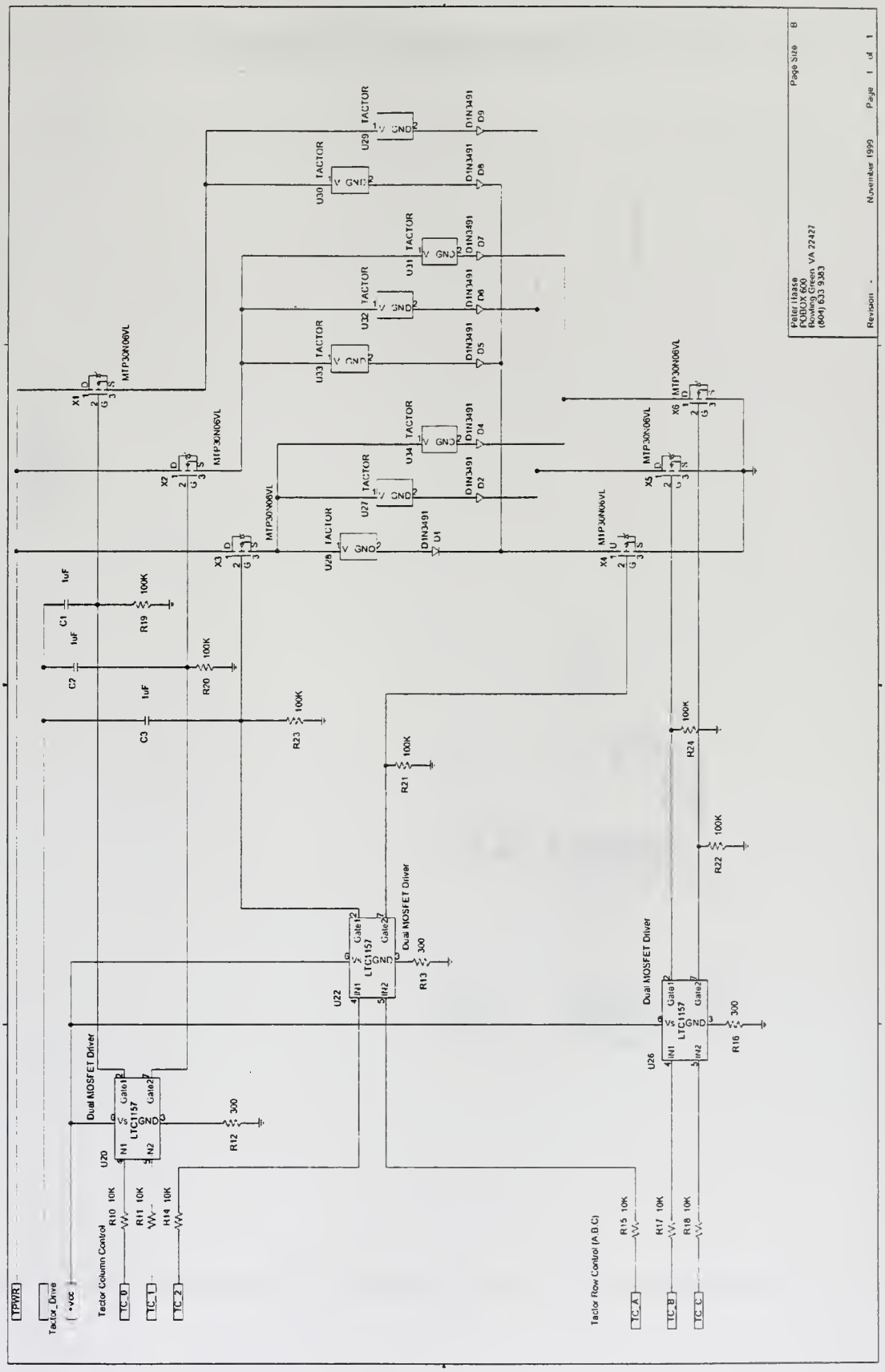
Appendix B – Memory Circuit



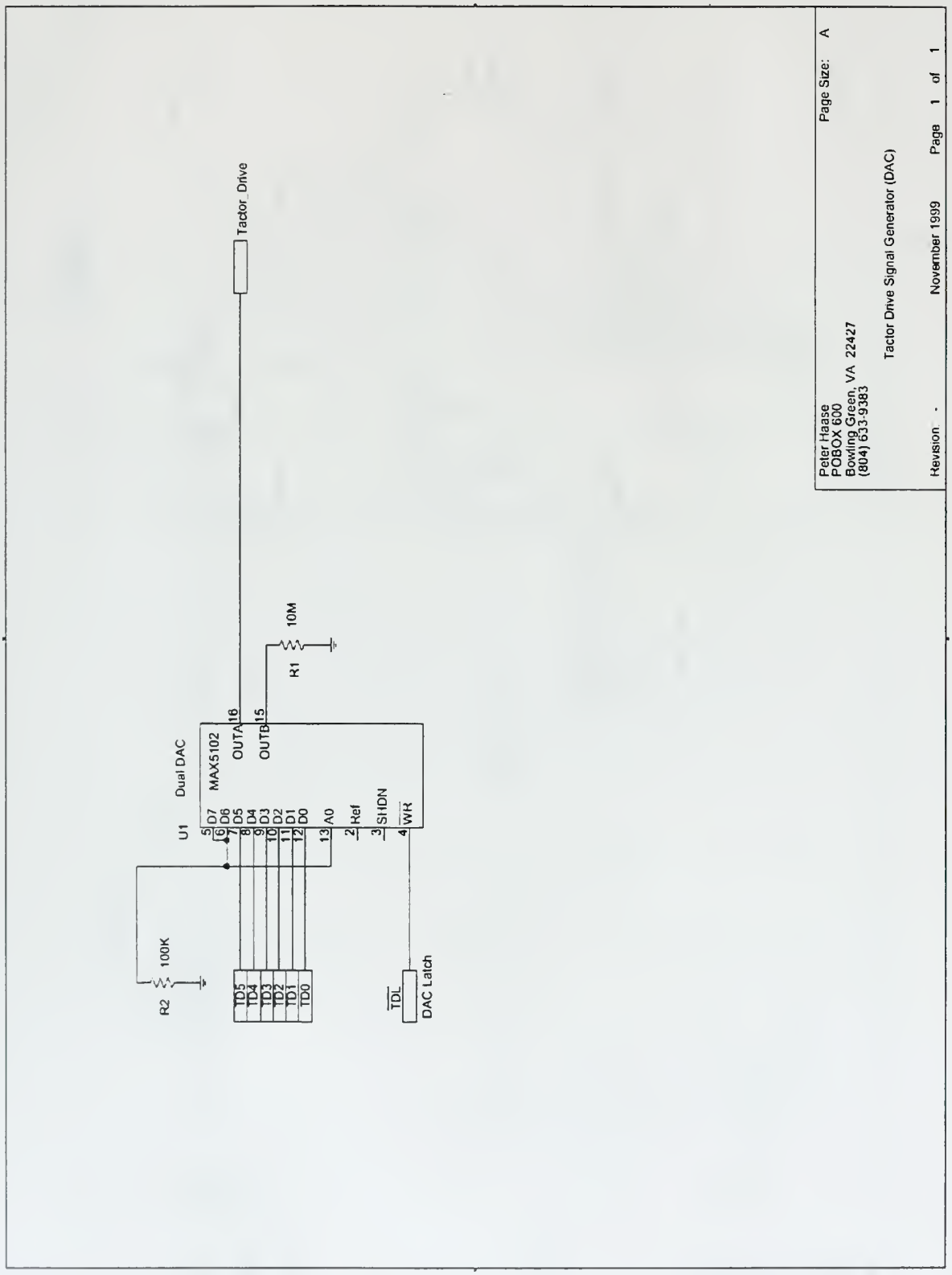
Appendix B – Power Circuit



Appendix B – Tactor Control Circuit

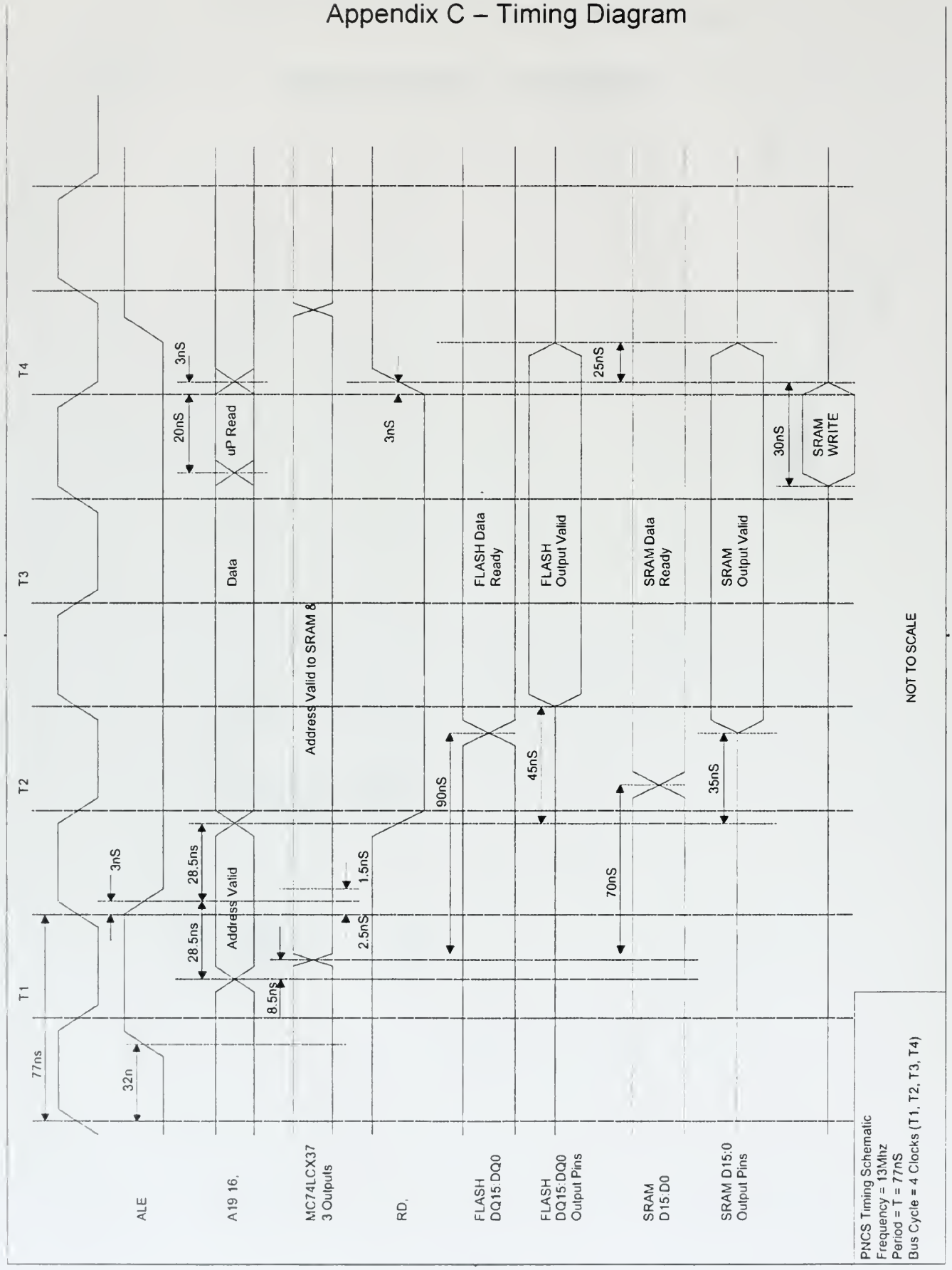


Appendix B – Tactor Drive Signal Generator



APPENDIX C – TIMING DIAGRAM

Appendix C – Timing Diagram

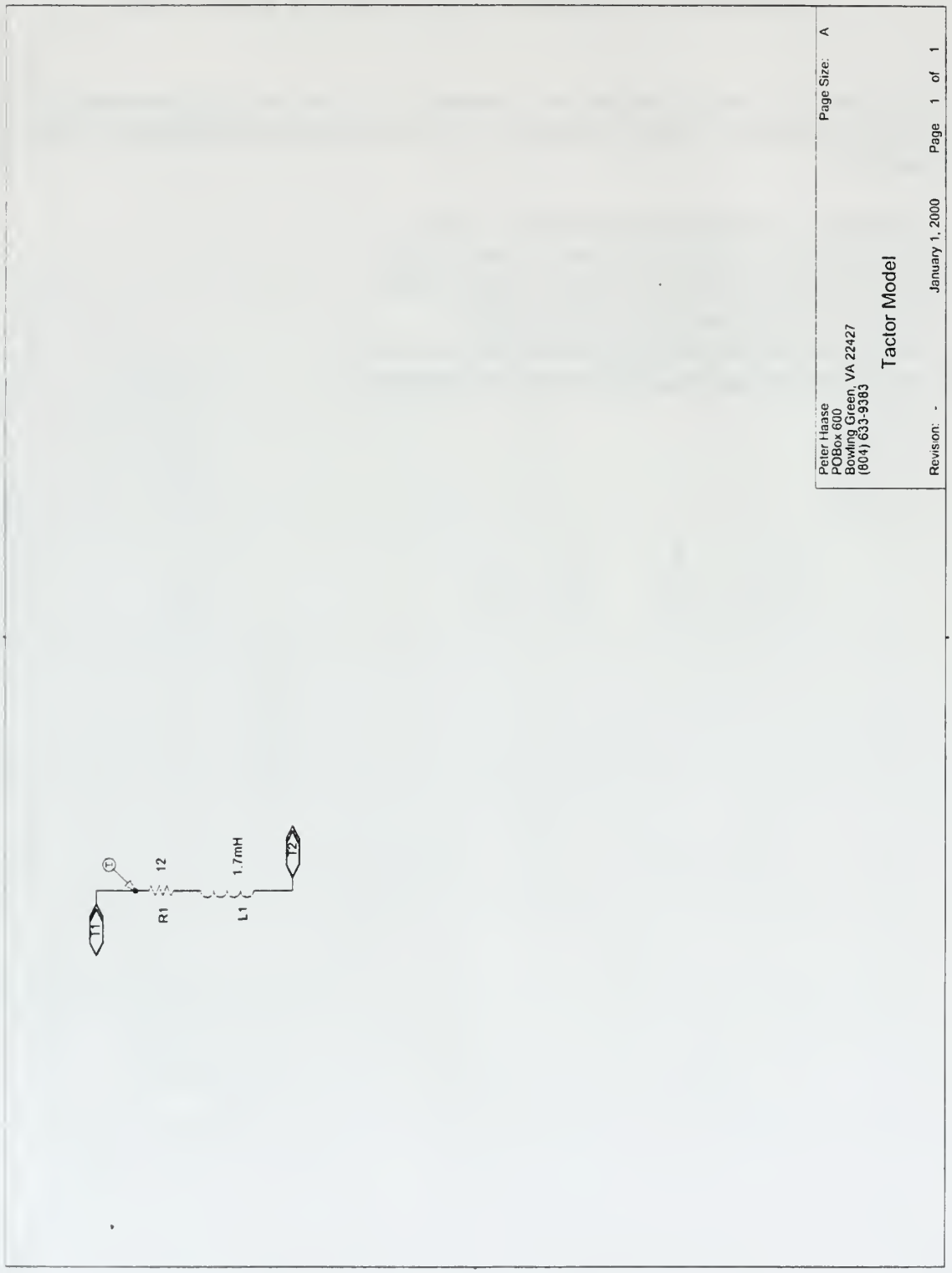


APPENDIX D – TACTOR DRIVER CIRCUIT SIMULATION

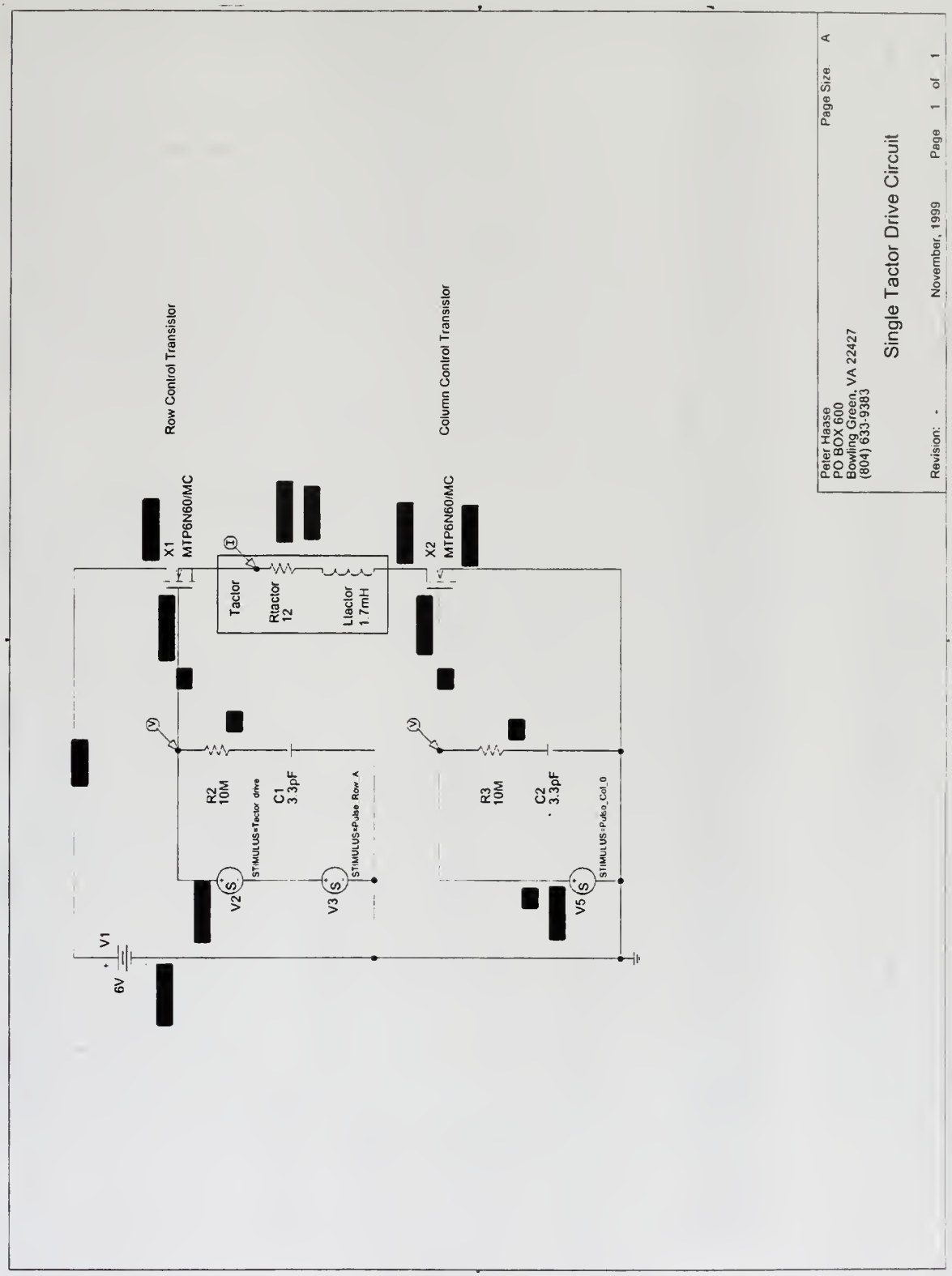
This appendix contains the source schematics and the output generated by Microsim DesignLab. The following is a list of the documents included in this appendix.

1. Schematic of the EAI tactor SPICE model
2. Schematic of a single EAI tactor driver circuit
3. Input Signals to the single tactor driver circuit
4. Output of the single tactor driver circuit
5. Schematic of the composite tactor driver circuit
6. Output of the composite tactor driver circuit

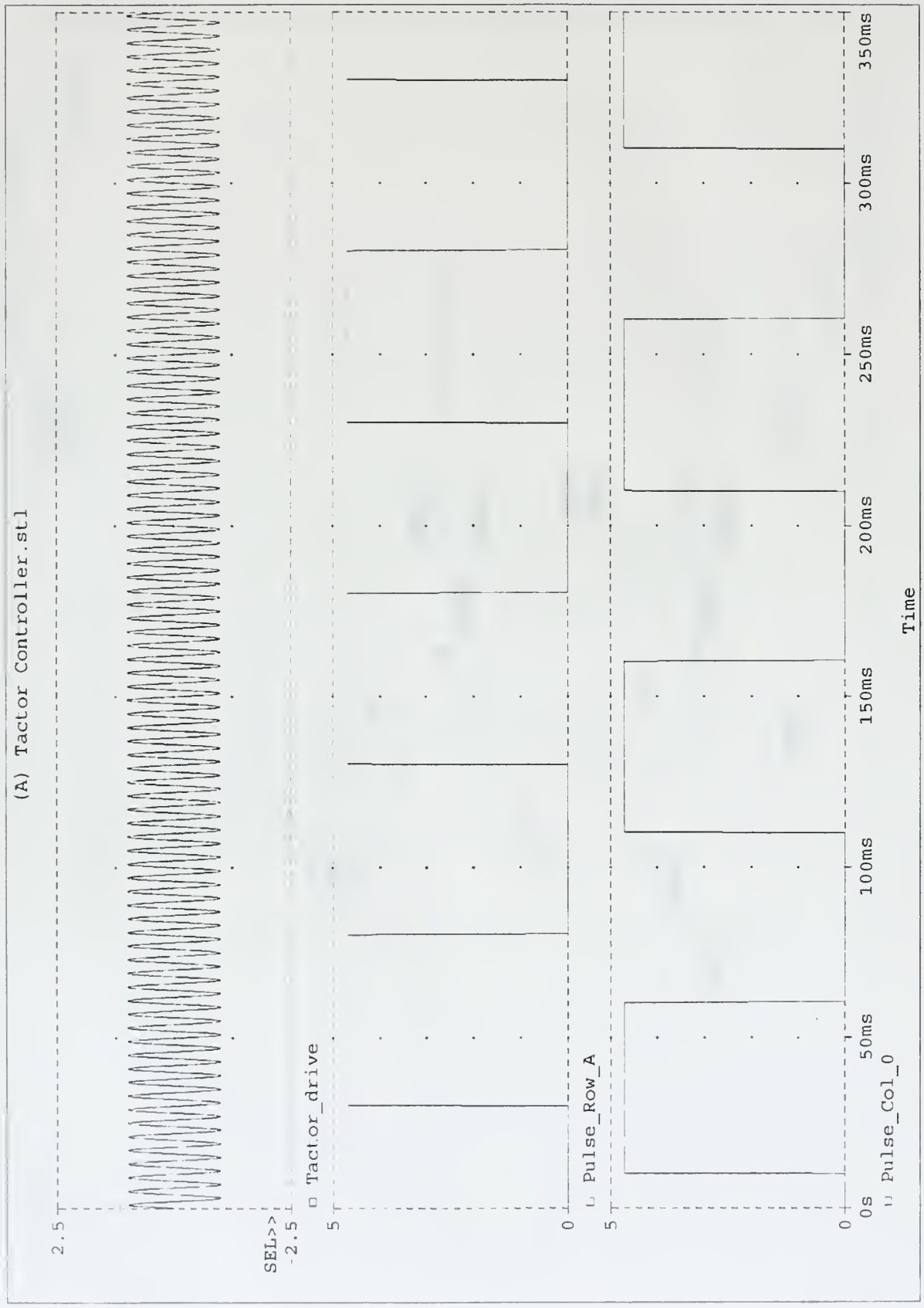
Appendix D – SPICE Model of the EAI Tactor



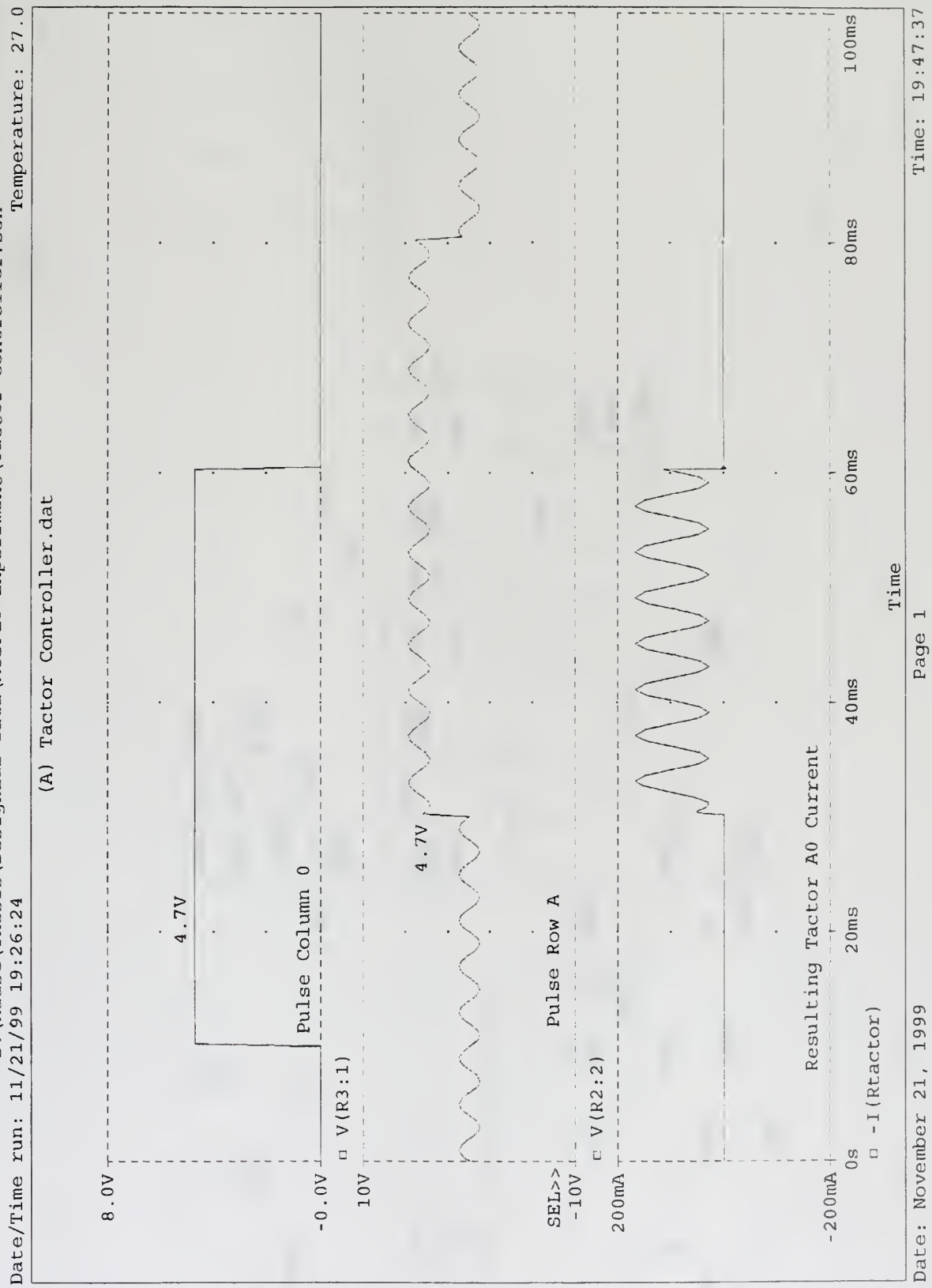
Appendix D – Single EAI Tactor Driver Circuit



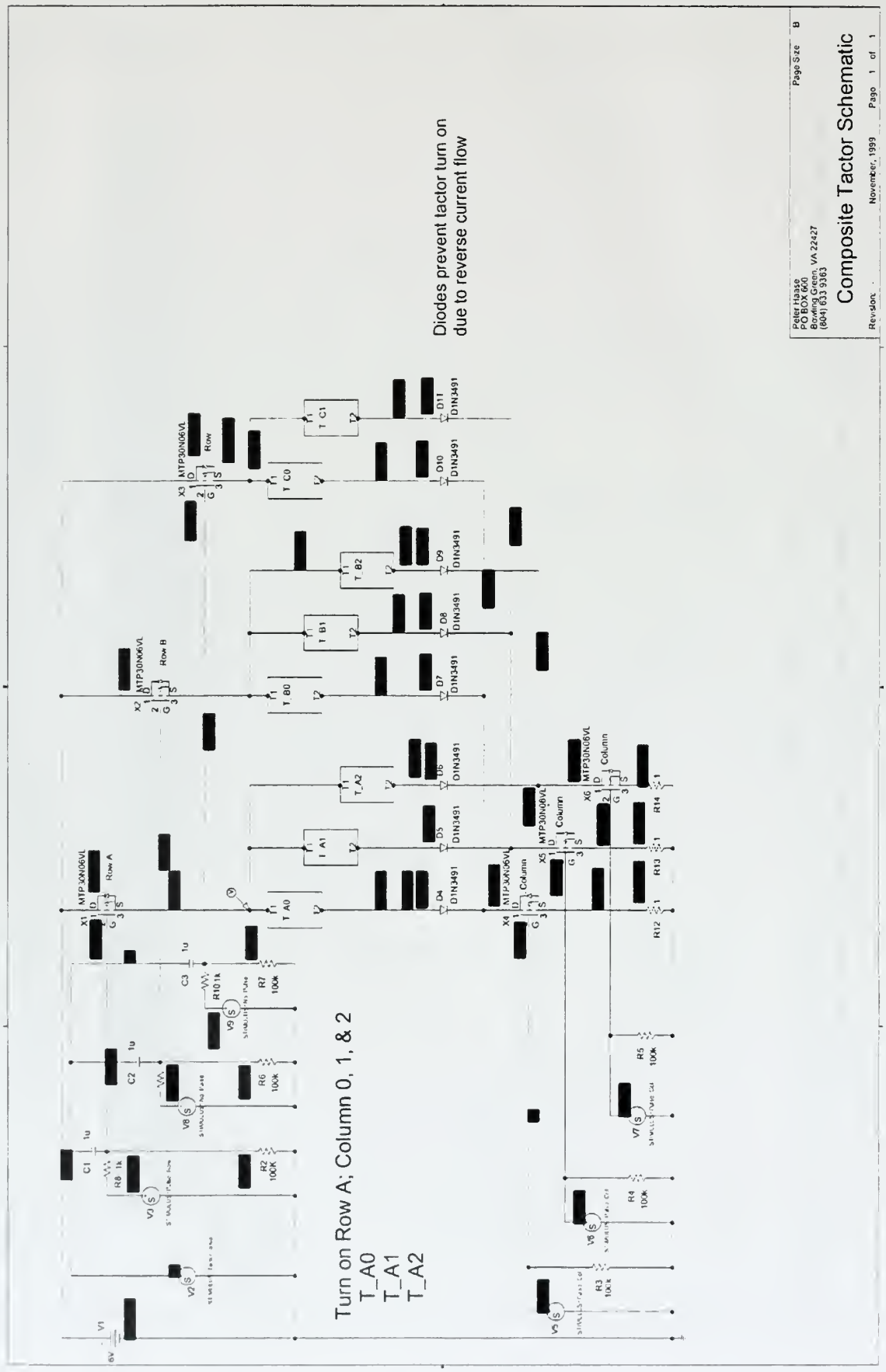
Appendix D – Tactor Driver Circuit Input Signals

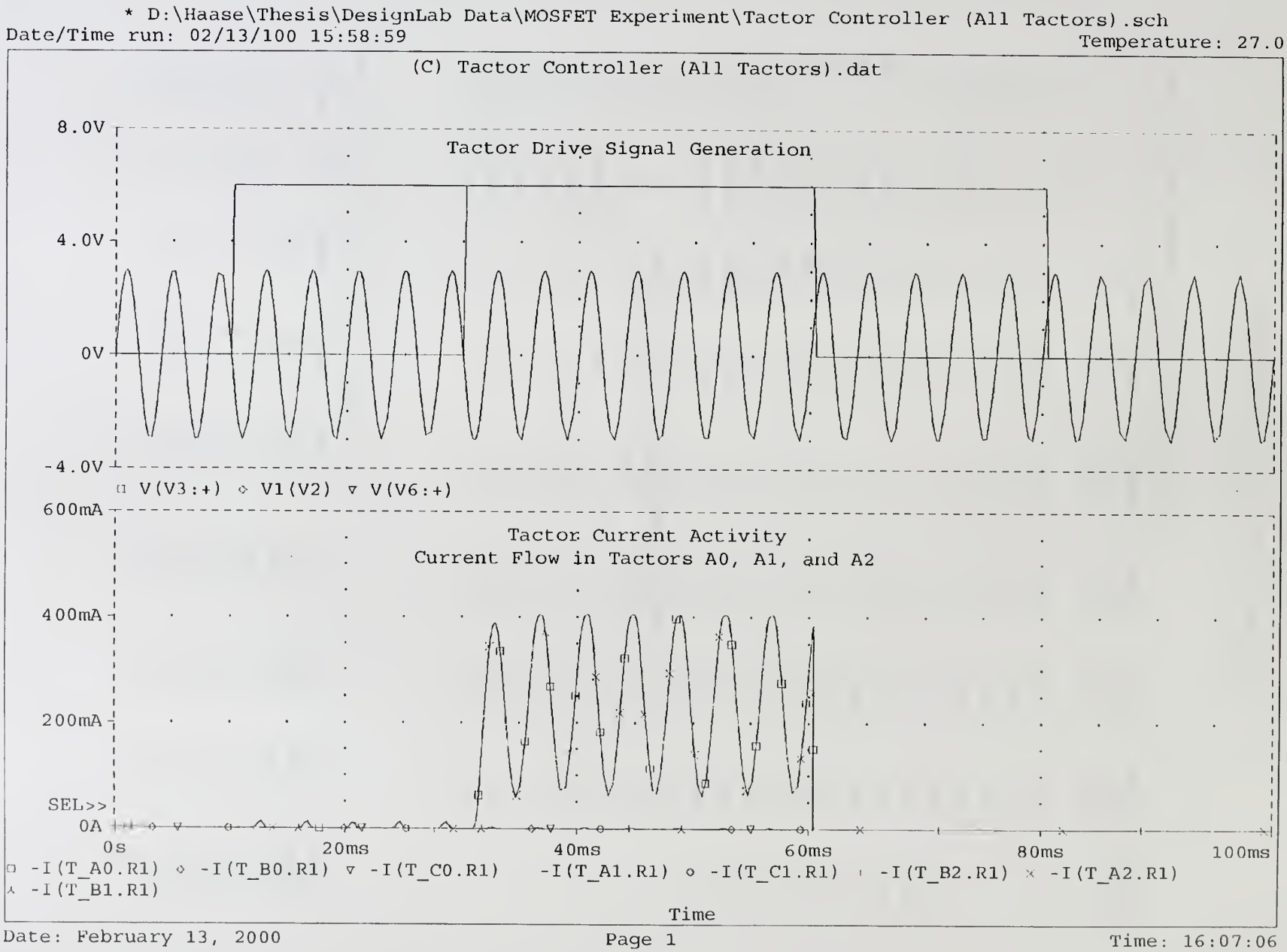


Appendix D – Output of Single Tactor Driver Circuit



Appendix D – Composite Tactor Driver Circuit




* D:\Haase\Thesis\DesignLab Data\MOSFET Experiment\Tactor Controller (All Tactors).sch
Date/Time run: 02/13/100 15:58:59
Temperature: 27.0
(C) Tactor Controller (All Tactors).dat
Tactor Drive Signal Generation
8.0V
4.0V
0V
-4.0V
V(V3:+) V1(V2) V(V6:+)
Tactor Current Activity
Current Flow in Tactors A0, A1, and A2
600mA
400mA
200mA
SEL>>
0A
0s
20ms
40ms
60ms
80ms
100ms
-I(T_A0.R1) -I(T_B0.R1) -I(T_C0.R1) -I(T_A1.R1) -I(T_C1.R1) -I(T_B2.R1) -I(T_A2.R1)
-I(T_B1.R1)
Time
Date: February 13, 2000
Page 1
Time: 16:07:06

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APPENDIX E – BATTERY TABLES

Table 26. Typical Alkaline Battery Characteristics.

Name	Size	Voltage (v)	Weight (g)	Diameter (mm)	Height (mm)	Length (mm)	Width (mm)	Capacity (mAh)
EN6	6 " Cylinder	1.5	482	66.7	170	N/A	N/A	
EN22	9V	9	45.6	N/A	46.4	26.5	17.5	
EN91	AA	1.5	23	14.5	50.5	N/A	N/A	
EN92	AAA	1.5	11.5	10.5	44.5	N/A	N/A	
EN132A	Button	3	18	17.1	33.4	N/A	N/A	
EN1A	Button	Stack	LR50	8.3	15.8	16.5	N/A	N/A
EN640A	Button	Stack	LR52	6	15.8	11.1	N/A	N/A
EN177A	Button	Stack	7LR44	14	12.95	47.15	N/A	N/A
EN133A	Button	Stack	3LR50	27	17.5	49.9	N/A	N/A
EN134A	Button	Stack	4LR50	36	17.1	66.55	N/A	N/A
EN164A	Button	Stack	4LR52	25.5	17.1	44.9	N/A	N/A
EN135A	Button	Stack	5LR50	45	17.1	83.2	N/A	N/A
EN165A	Button	Stack	5LR52	31.5	17.1	56.15	N/A	N/A
EN175A	Button	Stack	5LR44	9.5	11.6	5.4	N/A	N/A
EN136A	Button	Stack	6LR50	54	17.1	99.8	N/A	N/A
EN93	C	1.5	66.2	26.2	50	N/A	N/A	
EN95	D	1.5	141.9	34.2	61.5	N/A	N/A	
EN539	J	6	30	N/A	48.5	35.55	9.2	
EN529	Lantern	6	885	N/A	115	27	66.7	
EN715	Lantern	7.5	2.3 Kg	N/A	97	184.2	103.2	
EN90	N	1.5	9	12	30.2	N/A	N/A	
EDL4A	Pack	6	99	N/A	50.3	56.4	14.4	
EDL4AS	Pack	6	99.7	N/A	50.3	63.9	14.4	
EDL6A	Pack	9	9	N/A	50.3	49.6	26.6	

Table 27. Typical NiCad Battery Characteristics.

Name	Size	Voltage (v)	Weight (g)	Diameter (mm)	Height (mm)	Length (mm)	Width (mm)	Capacity (mAh)
CH22	9V	7.2	43	N/A	48.5	26.5	16.9	120
CH15	AA	1.2	22.7	14.5	50.5	N/A	N/A	650
CH12	AAA	1.2	9.5	10.5	44.5	N/A	N/A	220
CH35	C	1.2	54	26.2	50	N/A	N/A	1800
CH4	D	1.2	135	34.2	61.5	N/A	N/A	4000
CH50	D	1.2	67	34.2	61.5	N/A	N/A	1800

Table 28. Typical NiMH Battery Characteristics.

Name	Size	Voltage (v)	Weight (g)	Diameter (mm)	Height (mm)	Length (mm)	Width (mm)	Capacity (mAh)
NH22	9V	7.2	41	N/A	48.5	26.5	16.9	150
NH15	AA	1.2	27	14.5	50.5	N/A	N/A	1200
NH12	AAA	1.2	12	10.5	44.5	N/A	N/A	550
NH35	C	1.2	60	26.2	50	N/A	N/A	2200
NH50	D	1.2	73	34.2	61.5	N/A	N/A	2200

APPENDIX F – TECHNICAL DATA SHEETS

All of the components used in this design are commercially available parts. Due the number of pages required to reproduce them, the actual data sheets are not included here. Rather, they are packaged together to make up the "PNCS Thesis: Combined Reference Document (CRD)." The CRD is included with the submission of this thesis as a separate document. The Intel 80C186EC/80L186EC User Manual is not included in the CRD due to its size. The following is a list of documents included in the CRD.

Engineering Acoustics
- C1-97 Vibrotactile Transducer

Linear Technologies
- LTC1157 3.3V Dual MOSFET Driver

ILSI
- 2mm x 6mm Family Crystal

Maxim Integrated Products
- MAX3221 RS-232 Transceiver with AutoShutdown
- MAX603/604 Linear Regulators
- MAX6316-6322 Supervisory Circuits
- MAX6816-6818 CMOS Switch Debouncer

Micron Technologies Incorporated
- MT28F400B3 Smart-3 FLASH MEMORY

Motorola
- MC74LCX373 Low-Voltage CMOS Octal Latch
- MTD3055VL N-Channel Enhancement Mode Power FET

Samsung
- KM616U4000C CMOS SRAM

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